



# SPEC CPU®2017 Integer Speed Result

Copyright 2017-2022 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS X210c M6 (Intel Xeon Silver 4310T, 2.30GHz)

SPECspeed®2017\_int\_base = 10.7

SPECspeed®2017\_int\_peak = Not Run

CPU2017 License: 9019

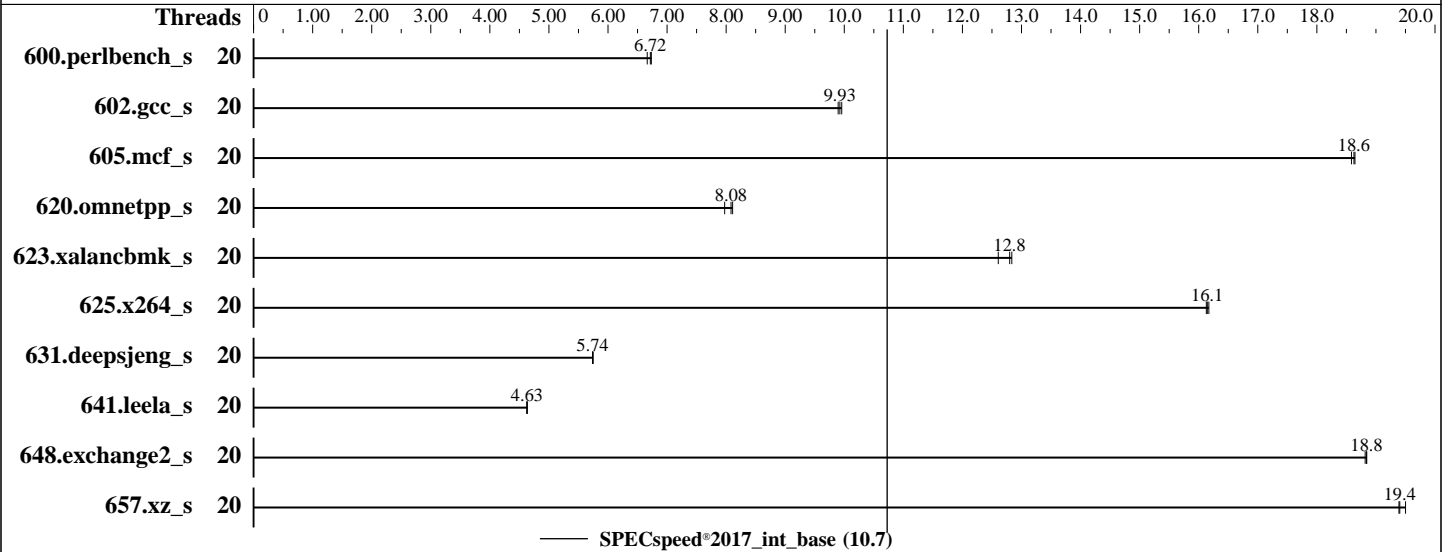
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Dec-2021

Hardware Availability: Sep-2021

Software Availability: Sep-2021



### Hardware

CPU Name: Intel Xeon Silver 4310T  
 Max MHz: 3400  
 Nominal: 2300  
 Enabled: 20 cores, 2 chips  
 Orderable: 1,2 Chips  
 Cache L1: 32 KB I + 48 KB D on chip per core  
 L2: 1.25 MB I+D on chip per core  
 L3: 15 MB I+D on chip per chip  
 Other: None  
 Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R, running at 2666)  
 Storage: 1 x 240 GB M.2 SSD SATA  
 Other: None

### Software

OS: SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default  
 Compiler: C/C++: Version 2021.4.0 of Intel oneAPI DPC++/C++ Compiler Build 20210924 for Linux; Fortran: Version 2021.4.0 of Intel Fortran Compiler Classic Build 20210910 for Linux;  
 Parallel: Yes  
 Firmware: Version 5.0.1d released Aug-2021  
 File System: btrfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: Not Applicable  
 Other: jemalloc memory allocator V5.0.1  
 Power Management: BIOS and OS set to prefer performance at the cost of additional power usage



# SPEC CPU®2017 Integer Speed Result

Copyright 2017-2022 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS X210c M6 (Intel Xeon Silver 4310T, 2.30GHz)

SPECspeed®2017\_int\_base = 10.7

SPECspeed®2017\_int\_peak = Not Run

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Dec-2021  
**Hardware Availability:** Sep-2021  
**Software Availability:** Sep-2021

## Results Table

Benchmark	Base								Peak							
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio		
600.perlbench_s	20	266	6.66	264	6.73	<b>264</b>	<b>6.72</b>									
602.gcc_s	20	<b>401</b>	<b>9.93</b>	402	9.90	400	9.96									
605.mcf_s	20	<b>253</b>	<b>18.6</b>	253	18.6	254	18.6									
620.omnetpp_s	20	<b>202</b>	<b>8.08</b>	201	8.11	205	7.97									
623.xalancbmk_s	20	112	12.6	110	12.8	<b>111</b>	<b>12.8</b>									
625.x264_s	20	109	16.2	<b>109</b>	<b>16.1</b>	109	16.1									
631.deepsjeng_s	20	249	5.75	<b>250</b>	<b>5.74</b>	250	5.74									
641.leela_s	20	368	4.63	<b>369</b>	<b>4.63</b>	369	4.63									
648.exchange2_s	20	156	18.8	156	18.8	<b>156</b>	<b>18.8</b>									
657.xz_s	20	317	19.5	<b>319</b>	<b>19.4</b>	319	19.4									

SPECspeed®2017\_int\_base = 10.7

SPECspeed®2017\_int\_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:

```
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH =
  "/home/intel/tbb/2021.4.0/env/./lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0//libfabric/lib:/home/intel/mpi/2021.4.0//lib/release:/home/intel/mpi/2021.4.0//lib:/home/intel/compiler/2021.4.0/linux/compiler/lib/intel64_lin:/home/intel/compiler/2021.4.0/linux/lib:/home/intel/clck/2021.4.0/lib/intel64:/home/cpu2017/je5.0.1-32"
MALLOCONF = "retain:true"
OMP_STACKSIZE = "192M"
```

## General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Redhat Enterprise Linux 8.0  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
sync; echo 3> /proc/sys/vm/drop\_caches  
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)

(Continued on next page)



# SPEC CPU®2017 Integer Speed Result

Copyright 2017-2022 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS X210c M6 (Intel Xeon Silver 4310T, 2.30GHz)

SPECspeed®2017\_int\_base = 10.7

SPECspeed®2017\_int\_peak = Not Run

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Dec-2021

**Hardware Availability:** Sep-2021

**Software Availability:** Sep-2021

### General Notes (Continued)

is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation

built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

### Platform Notes

BIOS Settings:

Adjacent Cache Line Prefetcher set to Disabled

DCU Streamer Prefetch set to Disabled

Sub NUMA Clustering set to Enabled

LLC Dead Line set to Disabled

Memory Refresh Rate set to 1x Refresh

ADDDC Sparing set to Disabled

Patrol Scrub set to Disabled

Intel Hyper-Threading Technology set to Disable

Processor C6 Report set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo

Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d

running on perf-blade5 Sun Dec 12 14:26:20 2021

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Silver 4310T CPU @ 2.30GHz

2 "physical id"s (chips)

20 "processors"

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

cpu cores : 10

siblings : 10

physical 0: cores 0 1 2 3 4 5 6 7 8 9

physical 1: cores 0 1 2 3 4 5 6 7 8 9

From lscpu from util-linux 2.33.1:

Architecture: x86\_64

CPU op-mode(s): 32-bit, 64-bit

Byte Order: Little Endian

Address sizes: 46 bits physical, 57 bits virtual

CPU(s): 20

On-line CPU(s) list: 0-19

(Continued on next page)



# SPEC CPU®2017 Integer Speed Result

Copyright 2017-2022 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS X210c M6 (Intel Xeon Silver 4310T, 2.30GHz)

SPECspeed®2017\_int\_base = 10.7

SPECspeed®2017\_int\_peak = Not Run

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Dec-2021

Hardware Availability: Sep-2021

Software Availability: Sep-2021

### Platform Notes (Continued)

```

Thread(s) per core: 1
Core(s) per socket: 10
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Silver 4310T CPU @ 2.30GHz
Stepping: 6
CPU MHz: 800.667
CPU max MHz: 3400.0000
CPU min MHz: 800.0000
BogoMIPS: 4600.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 15360K
NUMA node0 CPU(s): 0-9
NUMA node1 CPU(s): 10-19
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single ssbd
mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad
fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f
avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha_ni
avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
cqm_mbm_local wbnoinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp
hwp_pkg_req avx512vbmi umip pku ospke avx512_vbmi2 gfni vaes vpclmulqdq avx512_vnni
avx512_bitalg tme avx512_vpopcntdq la57 rdpid md_clear pconfig flush_l1d
arch_capabilities

```

```

/proc/cpuinfo cache data
cache size : 15360 KB

```

From numactl --hardware

WARNING: a numactl 'node' might or might not correspond to a physical chip.

```

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9
node 0 size: 1031748 MB
node 0 free: 1031199 MB
node 1 cpus: 10 11 12 13 14 15 16 17 18 19
node 1 size: 1032185 MB
node 1 free: 1031833 MB

```

(Continued on next page)



# SPEC CPU®2017 Integer Speed Result

Copyright 2017-2022 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS X210c M6 (Intel Xeon Silver 4310T, 2.30GHz)

SPECspeed®2017\_int\_base = 10.7

SPECspeed®2017\_int\_peak = Not Run

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Dec-2021  
**Hardware Availability:** Sep-2021  
**Software Availability:** Sep-2021

### Platform Notes (Continued)

node distances:

```
node 0 1
0: 10 20
1: 20 10
```

From /proc/meminfo

```
MemTotal: 2113469136 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
```

/sys/devices/system/cpu/cpu\*/cpufreq/scaling\_governor has performance

From /etc/\*release\* /etc/\*version\*

```
os-release:
NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"
```

uname -a:

```
Linux perf-blade5 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba)
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

```
CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected
```

run-level 3 Dec 12 14:22

(Continued on next page)



# SPEC CPU®2017 Integer Speed Result

Copyright 2017-2022 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS X210c M6 (Intel Xeon Silver 4310T, 2.30GHz)

SPECspeed®2017\_int\_base = 10.7

SPECspeed®2017\_int\_peak = Not Run

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Dec-2021

**Hardware Availability:** Sep-2021

**Software Availability:** Sep-2021

## Platform Notes (Continued)

SPEC is set to: /home/cpu2017

Filesystem	Type	Size	Used	Avail	Use%	Mounted on
/dev/sdb2	btrfs	224G	52G	172G	24%	/home

From /sys/devices/virtual/dmi/id

```
Vendor:      Cisco Systems Inc
Product:    UCSX-210C-M6
Serial:     FCH250671LG
```

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:

32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200, configured at 2666

BIOS:

```
BIOS Vendor:    Cisco Systems, Inc.
BIOS Version:   X210M6.5.0.1d.0.0816211754
BIOS Date:      08/16/2021
BIOS Revision:  5.22
```

(End of data from sysinfo program)

## Compiler Version Notes

```
=====  
C      | 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base)  
      | 625.x264_s(base) 657.xz_s(base)  
-----
```

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.4.0 Build 20210924  
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.

```
=====  
C++    | 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)  
      | 641.leela_s(base)  
-----
```

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.4.0 Build 20210924  
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.

```
=====  
Fortran | 648.exchange2_s(base)  
-----
```

(Continued on next page)



# SPEC CPU®2017 Integer Speed Result

Copyright 2017-2022 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS X210c M6 (Intel Xeon Silver 4310T, 2.30GHz)

SPECspeed®2017\_int\_base = 10.7

SPECspeed®2017\_int\_peak = Not Run

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Dec-2021

**Hardware Availability:** Sep-2021

**Software Availability:** Sep-2021

## Compiler Version Notes (Continued)

-----  
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.4.0 Build 20210910\_000000  
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.  
-----

## Base Compiler Invocation

C benchmarks:

icx

C++ benchmarks:

icpx

Fortran benchmarks:

ifort

## Base Portability Flags

600.perlbench\_s: -DSPEC\_LP64 -DSPEC\_LINUX\_X64  
602.gcc\_s: -DSPEC\_LP64  
605.mcf\_s: -DSPEC\_LP64  
620.omnetpp\_s: -DSPEC\_LP64  
623.xalancbmk\_s: -DSPEC\_LP64 -DSPEC\_LINUX  
625.x264\_s: -DSPEC\_LP64  
631.deepsjeng\_s: -DSPEC\_LP64  
641.leela\_s: -DSPEC\_LP64  
648.exchange2\_s: -DSPEC\_LP64  
657.xz\_s: -DSPEC\_LP64

## Base Optimization Flags

C benchmarks:

-DSPEC\_OPENMP -std=c11 -m64 -fiopenmp -Wl,-z,muldefs -xCORE-AVX512  
-O3 -ffast-math -flto -mfpmath=sse -funroll-loops  
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries  
-L/home/cpu2017/je5.0.1-64 -ljemalloc

C++ benchmarks:

-DSPEC\_OPENMP -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math  
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4

(Continued on next page)



# SPEC CPU®2017 Integer Speed Result

Copyright 2017-2022 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS X210c M6 (Intel Xeon Silver 4310T, 2.30GHz)

SPECspeed®2017\_int\_base = 10.7

SPECspeed®2017\_int\_peak = Not Run

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Dec-2021

**Hardware Availability:** Sep-2021

**Software Availability:** Sep-2021

## Base Optimization Flags (Continued)

C++ benchmarks (continued):

```
-mbranches-within-32B-boundaries  
-L/home/intel/compiler/2021.4.0/linux/compiler/lib/intel64_lin/  
-lqkmalloc
```

Fortran benchmarks:

```
-m64 -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-mem-layout-trans=4  
-nostandard-realloc-lhs -align array32byte -auto  
-mbranches-within-32B-boundaries
```

The flags files that were used to format this result can be browsed at

[http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64\\_revA.2021-12-22.html](http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.2021-12-22.html)

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-rev1.html>

You can also download the XML flags sources by saving the following links:

[http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64\\_revA.2021-12-22.xml](http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.2021-12-22.xml)

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-rev1.xml>

SPEC CPU and SPECspeed are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact [info@spec.org](mailto:info@spec.org).

Tested with SPEC CPU®2017 v1.1.8 on 2021-12-12 17:26:19-0500.

Report generated on 2022-01-05 13:36:48 by CPU2017 PDF formatter v6442.

Originally published on 2022-01-04.