



SPEC CPU®2017 Integer Speed Result

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Tyrone Systems

(Test Sponsor: Netweb Pte Ltd)

Tyrone Camarero DIT400TR-28R
(2.10 GHz, Intel Xeon Gold 5218R)

SPECspeed®2017_int_base = 8.65

SPECspeed®2017_int_peak = 8.85

CPU2017 License: 006042

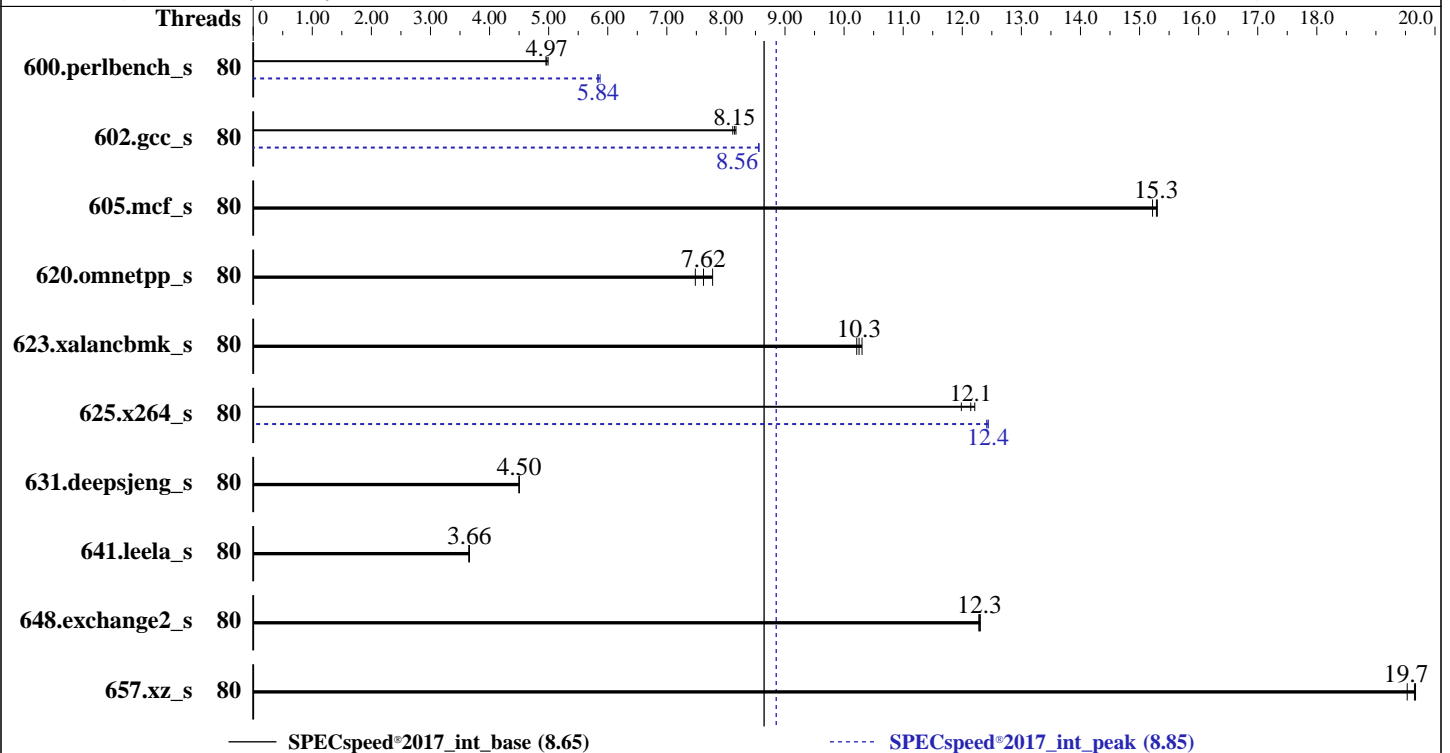
Test Sponsor: Netweb Pte Ltd

Tested by: Tyrone Systems

Test Date: Jul-2021

Hardware Availability: Feb-2020

Software Availability: Jun-2021



Hardware

CPU Name: Intel Xeon Gold 5218R
 Max MHz: 4000
 Nominal: 2100
 Enabled: 40 cores, 2 chips, 2 threads/core
 Orderable: 1,2 Chips
 Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 27.5 MB I+D on chip per chip
 Other: None
 Memory: 384 GB (12 x 32 GB 2Rx4 PC4-2933P-R, running at 2666)
 Storage: 1 x 480 GB SATA SSD
 Other: None

Software

OS: CentOS Linux release 8.4.2105
 Kernel 4.18.0-305.3.1.el8.x86_64
 Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux;
 Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;
 C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux;
 Parallel: Yes
 Firmware: Version 3.4a released Jan-2021
 File System: xfs
 System State: Run level 3 (multi-user)
 Base Pointers: 64-bit
 Peak Pointers: 64-bit
 Other: jemalloc memory allocator V5.0.1
 Power Management: BIOS set to prefer performance at the cost of additional power usage.



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Results Table

Benchmark	Base							Peak						
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
600.perlbench_s	80	357	4.97	356	4.99	358	4.95	80	304	5.83	304	5.84	302	5.87
602.gcc_s	80	491	8.12	487	8.17	489	8.15	80	465	8.56	465	8.56	465	8.56
605.mcf_s	80	310	15.2	309	15.3	309	15.3	80	310	15.2	309	15.3	309	15.3
620.omnetpp_s	80	218	7.48	214	7.62	210	7.78	80	218	7.48	214	7.62	210	7.78
623.xalancbmk_s	80	139	10.2	138	10.3	138	10.3	80	139	10.2	138	10.3	138	10.3
625.x264_s	80	144	12.2	147	12.0	145	12.1	80	142	12.4	142	12.4	142	12.4
631.deepsjeng_s	80	318	4.50	318	4.50	318	4.50	80	318	4.50	318	4.50	318	4.50
641.leela_s	80	466	3.66	466	3.66	468	3.65	80	466	3.66	466	3.66	468	3.65
648.exchange2_s	80	239	12.3	239	12.3	239	12.3	80	239	12.3	239	12.3	239	12.3
657.xz_s	80	314	19.7	317	19.5	315	19.7	80	314	19.7	317	19.5	315	19.7

SPECspeed®2017_int_base = **8.65**

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:

```
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOCONF = "retain:true"
OMP_STACKSIZE = "192M"
```

General Notes

```
Binaries compiled locally by Netweb
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

```
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
```

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General Notes (Continued)

sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

Platform Notes

BIOS Settings:

Power Technology set to Custom

Power Performance Tuning set to BIOS Controls EPB

ENERGY_PERF_BIAS_CFG mode set to Performance

LLC Dead Line Alloc set to Disable

Sysinfo program /home/cpu2017/bin/sysinfo

Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d

running on localhost.localdomain Wed Jul 28 21:13:05 2021

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Gold 5218R CPU @ 2.10GHz

2 "physical id"s (chips)

80 "processors"

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

cpu cores : 20

siblings : 40

physical 0: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28

physical 1: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28

From lscpu from util-linux 2.32.1:

Architecture: x86_64

CPU op-mode(s): 32-bit, 64-bit

Byte Order: Little Endian

CPU(s): 80

On-line CPU(s) list: 0-79

Thread(s) per core: 2

Core(s) per socket: 20

Socket(s): 2

NUMA node(s): 2

Vendor ID: GenuineIntel

BIOS Vendor ID: Intel(R) Corporation

CPU family: 6

Model: 85

Model name: Intel(R) Xeon(R) Gold 5218R CPU @ 2.10GHz

BIOS Model name: Intel(R) Xeon(R) Gold 5218R CPU @ 2.10GHz

Stepping: 7

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Platform Notes (Continued)

```

CPU MHz:                2900.284
CPU max MHz:            4000.0000
CPU min MHz:            800.0000
BogoMIPS:               4200.00
Virtualization:         VT-x
L1d cache:              32K
L1i cache:              32K
L2 cache:               1024K
L3 cache:               28160K
NUMA node0 CPU(s):     0-19,40-59
NUMA node1 CPU(s):     20-39,60-79
Flags:                  fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpperf pni pclmulqdq dtes64 ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm
pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c
rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single
intel_ppin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority ept
vpid ept_ad fsgsbase tsc_adjust bmil hle avx2 smep bmi2 erms invpcid cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
dtherm ida arat pln pts pku ospke avx512_vnni md_clear flush_lld arch_capabilities

```

```

/proc/cpuinfo cache data
cache size : 28160 KB

```

From numactl --hardware

WARNING: a numactl 'node' might or might not correspond to a physical chip.

```

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 40 41 42 43 44 45 46 47
48 49 50 51 52 53 54 55 56 57 58 59
node 0 size: 192115 MB
node 0 free: 150297 MB
node 1 cpus: 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 60 61 62 63 64
65 66 67 68 69 70 71 72 73 74 75 76 77 78 79
node 1 size: 193489 MB
node 1 free: 160148 MB
node distances:
node  0  1
  0:  10  21
  1:  21  10

```

From /proc/meminfo

```

MemTotal:        394859744 kB
HugePages_Total: 0
Hugepagesize:    2048 kB

```

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Platform Notes (Continued)

```

/sbin/tuned-adm active
  Current active profile: throughput-performance

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has
performance

From /etc/*release* /etc/*version*
centos-release: CentOS Linux release 8.4.2105
centos-release-upstream: Derived from Red Hat Enterprise Linux 8.4
os-release:
  NAME="CentOS Linux"
  VERSION="8"
  ID="centos"
  ID_LIKE="rhel fedora"
  VERSION_ID="8"
  PLATFORM_ID="platform:el8"
  PRETTY_NAME="CentOS Linux 8"
  ANSI_COLOR="0;31"
redhat-release: CentOS Linux release 8.4.2105
system-release: CentOS Linux release 8.4.2105
system-release-cpe: cpe:/o:centos:centos:8

uname -a:
Linux localhost.localdomain 4.18.0-305.3.1.el8.x86_64 #1 SMP Tue Jun 1 16:14:33 UTC
2021 x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit):          KVM: Mitigation: Split huge pages
CVE-2018-3620 (L1 Terminal Fault):      Not affected
Microarchitectural Data Sampling:      Not affected
CVE-2017-5754 (Meltdown):              Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store
Bypass disabled via prctl and
seccomp
CVE-2017-5753 (Spectre variant 1):      Mitigation: usercopy/swapgs
barriers and __user pointer
sanitization
CVE-2017-5715 (Spectre variant 2):      Mitigation: Enhanced IBRS, IBPB:
conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Mitigation: TSX disabled

run-level 3 Jul 27 05:52

SPEC is set to: /home/cpu2017
Filesystem      Type  Size  Used Avail Use% Mounted on

```

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Platform Notes (Continued)

```
/dev/mapper/cl-home xfs 372G 57G 315G 16% /home
```

```
From /sys/devices/virtual/dmi/id
Vendor: Tyrone Systems
Product: Tyrone Camarero DS400TR-28R
Serial: 0123456789
```

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
12x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2666

BIOS:
BIOS Vendor: American Megatrends Inc.
BIOS Version: 3.4a
BIOS Date: 01/07/2021
BIOS Revision: 5.14

(End of data from sysinfo program)

Compiler Version Notes

```
=====  
C | 600.perlbench_s(peak)  
-----
```

```
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)  
64, Version 2021.1 Build 20201112_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
-----
```

```
=====  
C | 600.perlbench_s(base) 602.gcc_s(base, peak) 605.mcf_s(base, peak)  
| 625.x264_s(base, peak) 657.xz_s(base, peak)  
-----
```

```
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
-----
```

```
=====  
C | 600.perlbench_s(peak)  
-----
```

```
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)  
64, Version 2021.1 Build 20201112_000000
```

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Compiler Version Notes (Continued)

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```
=====  
C      | 600.perlbench_s(base) 602.gcc_s(base, peak) 605.mcf_s(base, peak)  
      | 625.x264_s(base, peak) 657.xz_s(base, peak)  
=====
```

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

```
=====  
C++   | 620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak)  
      | 631.deepsjeng_s(base, peak) 641.leela_s(base, peak)  
=====
```

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

```
=====  
Fortran | 648.exchange2_s(base, peak)  
=====
```

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000

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Base Compiler Invocation

C benchmarks:

icx

C++ benchmarks:

icpx

Fortran benchmarks:

ifort

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64

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Base Portability Flags (Continued)

```
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64
```

Base Optimization Flags

C benchmarks:

```
-DSPEC_OPENMP -std=c11 -m64 -fiopenmp -Wl,-z,muldefs -xCORE-AVX512
-O3 -ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

C++ benchmarks:

```
-DSPEC_OPENMP -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin/
-lqkmalloc
```

Fortran benchmarks:

```
-m64 -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte
-mbranches-within-32B-boundaries
```

Peak Compiler Invocation

C benchmarks (except as noted below):

icx

600.perlbench_s: icc

C++ benchmarks:

icpx

Fortran benchmarks:

ifort



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Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

```
600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-mbranches-within-32B-boundaries
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

```
602.gcc_s: -m64 -std=c11 -Wl,-z,muldefs -fprofile-generate(pass 1)
-fprofile-use=default.profddata(pass 2) -xCORE-AVX512 -flto
-Ofast(pass 1) -O3 -ffast-math -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

605.mcf_s: basepeak = yes

```
625.x264_s: -DSPEC_OPENNMP -fiopenmp -std=c11 -m64 -Wl,-z,muldefs
-xCORE-AVX512 -flto -O3 -ffast-math
-qopt-mem-layout-trans=4 -fno-alias
-mbranches-within-32B-boundaries
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

657.xz_s: basepeak = yes

C++ benchmarks:

620.omnetpp_s: basepeak = yes

623.xalancbmk_s: basepeak = yes

631.deepsjeng_s: basepeak = yes

641.leela_s: basepeak = yes

Fortran benchmarks:

648.exchange2_s: basepeak = yes



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The flags files that were used to format this result can be browsed at

http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.html

<http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revI.html>

You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml

<http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revI.xml>

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