



SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8276L, 2.20GHz)

SPECspeed®2017_fp_base = 148

SPECspeed®2017_fp_peak = Not Run

CPU2017 License: 9019

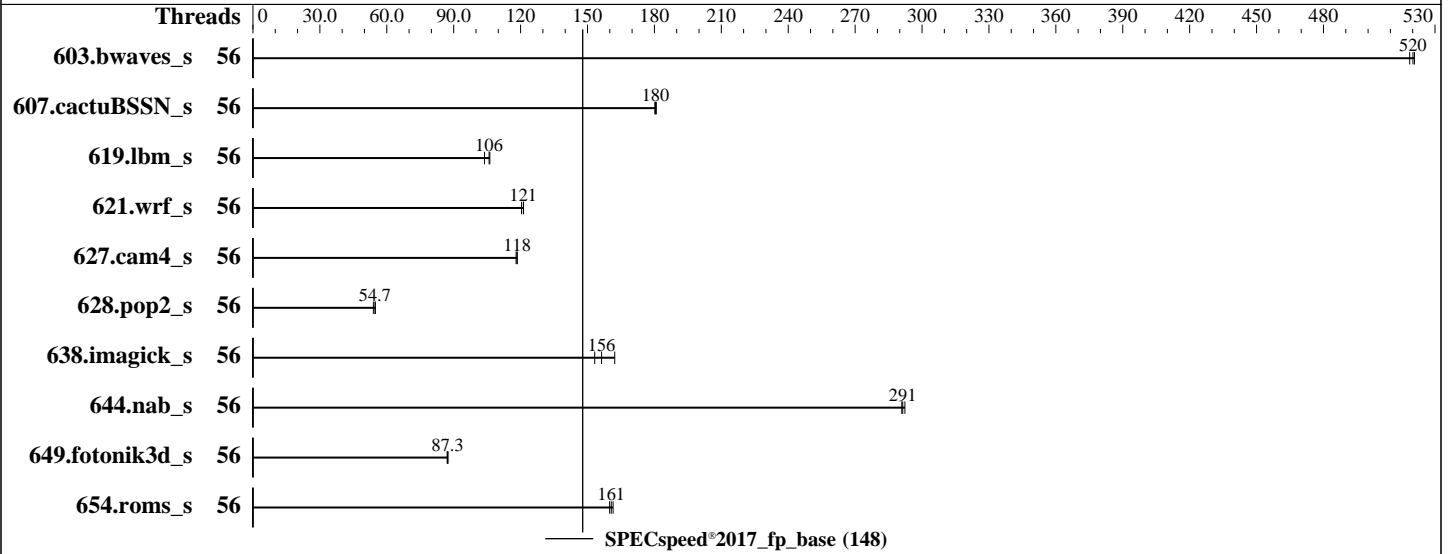
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2019

Hardware Availability: Apr-2019

Software Availability: May-2019



Hardware

CPU Name: Intel Xeon Platinum 8276L
 Max MHz: 4000
 Nominal: 2200
 Enabled: 56 cores, 2 chips
 Orderable: 1,2 chips
 Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 38.5 MB I+D on chip per chip
 Other: None
 Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
 Storage: 1 x 240G SSD SATA
 Other: None

Software

OS: SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
 Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
 Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
 Parallel: Yes
 Firmware: Version 4.0.4b released Apr-2019
 File System: btrfs
 System State: Run level 3 (multi-user)
 Base Pointers: 64-bit
 Peak Pointers: Not Applicable
 Other: None
 Power Management: --



SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8276L, 2.20GHz)

SPECspeed®2017_fp_base = 148

SPECspeed®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Results Table

| Benchmark | Base | | | | | | | Peak | | | | | | |
|-----------------|---------|-------------|------------|------------|-------------|-------------|-------------|---------|---------|-------|---------|-------|---------|-------|
| | Threads | Seconds | Ratio | Seconds | Ratio | Seconds | Ratio | Threads | Seconds | Ratio | Seconds | Ratio | Seconds | Ratio |
| 603.bwaves_s | 56 | 113 | 521 | 114 | 519 | 113 | 520 | | | | | | | |
| 607.cactuBSSN_s | 56 | 92.4 | 180 | 92.2 | 181 | 92.5 | 180 | | | | | | | |
| 619.lbm_s | 56 | 50.5 | 104 | 49.3 | 106 | 49.5 | 106 | | | | | | | |
| 621.wrf_s | 56 | 109 | 121 | 110 | 120 | 109 | 121 | | | | | | | |
| 627.cam4_s | 56 | 75.1 | 118 | 74.8 | 118 | 74.8 | 118 | | | | | | | |
| 628.pop2_s | 56 | 216 | 54.9 | 220 | 54.0 | 217 | 54.7 | | | | | | | |
| 638.imagick_s | 56 | 92.3 | 156 | 88.9 | 162 | 94.1 | 153 | | | | | | | |
| 644.nab_s | 56 | 59.8 | 292 | 60.1 | 291 | 60.0 | 291 | | | | | | | |
| 649.fotonik3d_s | 56 | 104 | 87.4 | 104 | 87.3 | 105 | 87.1 | | | | | | | |
| 654.roms_s | 56 | 98.0 | 161 | 98.5 | 160 | 97.5 | 161 | | | | | | | |

SPECspeed®2017_fp_base = 148

SPECspeed®2017_fp_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:

```
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"
```

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default

Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise

(Continued on next page)



SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8276L, 2.20GHz)

SPECspeed®2017_fp_base = 148

SPECspeed®2017_fp_peak = Not Run

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2019

Hardware Availability: Apr-2019

Software Availability: May-2019

Platform Notes (Continued)

Power Performance Tuning set to OS Controls
 SNC set to Disabled
 IMC Interleaving set to Auto
 Sysinfo program /home/cpu2017/bin/sysinfo
 Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
 running on linux-bo6o Fri Sep 6 14:22:10 2019

SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

```
From /proc/cpuinfo
model name      : Intel(R) Xeon(R) Platinum 8276L CPU @ 2.20GHz
 2 "physical id"s (chips)
 56 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores    : 28
  siblings    : 28
 physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27
                28 29 30
 physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27
                28 29 30
```

```
From lscpu:
Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Byte Order:             Little Endian
CPU(s):                 56
On-line CPU(s) list:   0-55
Thread(s) per core:    1
Core(s) per socket:    28
Socket(s):              2
NUMA node(s):          2
Vendor ID:              GenuineIntel
CPU family:             6
Model:                  85
Model name:             Intel(R) Xeon(R) Platinum 8276L CPU @ 2.20GHz
Stepping:               7
CPU MHz:                2200.000
CPU max MHz:           4000.0000
CPU min MHz:           1000.0000
BogoMIPS:               4400.00
Virtualization:        VT-x
L1d cache:              32K
L1i cache:              32K
L2 cache:               1024K
```

(Continued on next page)



SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8276L, 2.20GHz)

SPECspeed®2017_fp_base = 148

SPECspeed®2017_fp_peak = Not Run

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2019

Hardware Availability: Apr-2019

Software Availability: May-2019

Platform Notes (Continued)

```

L3 cache:                39424K
NUMA node0 CPU(s):      0-27
NUMA node1 CPU(s):      28-55
Flags:                    fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdp_l3 invpcid_single intel_ppin mba tpr_shadow vnmi flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ssbd

```

```

/proc/cpuinfo cache data
cache size : 39424 KB

```

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
node 0 size: 385426 MB
node 0 free: 383755 MB
node 1 cpus: 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52
53 54 55
node 1 size: 387043 MB
node 1 free: 379167 MB
node distances:
node    0    1
 0:    10    21
 1:    21    10

```

```

From /proc/meminfo
MemTotal:        791009524 kB
HugePages_Total:    0
Hugepagesize:     2048 kB

```

```

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"

```

(Continued on next page)



SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8276L, 2.20GHz)

SPECspeed®2017_fp_base = 148

SPECspeed®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

```
ANSI_COLOR="0;32"  
CPE_NAME="cpe:/o:suse:sles:15"
```

```
uname -a:  
Linux linux-bo6o 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)  
x86_64 x86_64 x86_64 GNU/Linux
```

```
run-level 3 Sep 6 08:36
```

```
SPEC is set to: /home/cpu2017  
Filesystem      Type  Size  Used Avail Use% Mounted on  
/dev/sdcl        btrfs 224G   22G  202G  10% /home
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

```
BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019  
Memory:  
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934
```

(End of data from sysinfo program)

Compiler Version Notes

```
=====  
C | 619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)  
=====
```

```
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
=====
```

```
=====  
C++, C, Fortran | 607.cactuBSSN_s(base)  
=====
```

```
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
=====
```

(Continued on next page)



SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8276L, 2.20GHz)

SPECspeed®2017_fp_base = 148

SPECspeed®2017_fp_peak = Not Run

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2019

Hardware Availability: Apr-2019

Software Availability: May-2019

Compiler Version Notes (Continued)

=====
Fortran | 603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)
=====

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

=====
Fortran, C | 621.wrf_s(base) 627.cam4_s(base) 628.pop2_s(base)
=====

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:

icc -m64 -std=c11

Fortran benchmarks:

ifort -m64

Benchmarks using both Fortran and C:

ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:

icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl

(Continued on next page)



SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8276L, 2.20GHz)

SPECspeed®2017_fp_base = 148

SPECspeed®2017_fp_peak = Not Run

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2019

Hardware Availability: Apr-2019

Software Availability: May-2019

Base Portability Flags (Continued)

638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:

-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs

Benchmarks using both Fortran and C:

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

Benchmarks using Fortran, C, and C++:

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic19.0ul-official-linux64.2019-07-09.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.2019-07-31.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic19.0ul-official-linux64.2019-07-09.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.2019-07-31.xml>

SPEC CPU and SPECspeed are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2019-09-06 17:22:10-0400.

Report generated on 2020-12-15 17:56:54 by CPU2017 PDF formatter v6255.

Originally published on 2019-10-01.