



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Silver 4112  
2.60 GHz)

SPECspeed®2017\_fp\_base = 45.0

SPECspeed®2017\_fp\_peak = Not Run

CPU2017 License: 9019

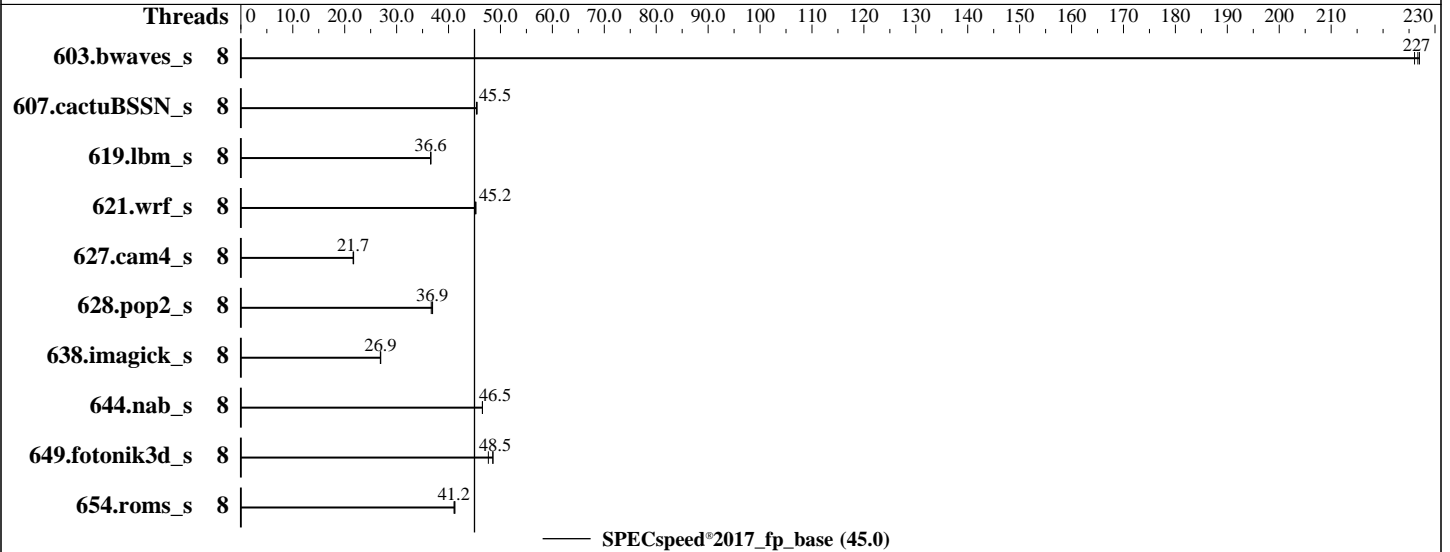
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Dec-2018

Hardware Availability: Aug-2017

Software Availability: Oct-2018



### Hardware

CPU Name: Intel Xeon Silver 4112  
 Max MHz: 3000  
 Nominal: 2600  
 Enabled: 8 cores, 2 chips  
 Orderable: 1,2 Chips  
 Cache L1: 32 KB I + 32 KB D on chip per core  
 L2: 1 MB I+D on chip per core  
 L3: 8.25 MB I+D on chip per chip  
 Other: None  
 Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2666V-R,  
 running at 2400)  
 Storage: 1 x 600G SAS 10K RPM  
 Other: None

### Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86\_64)  
 4.4.120-92.70-default  
 Compiler: C/C++: Version 19.0.1.144 of Intel C/C++  
 Compiler for Linux;  
 Fortran: Version 19.0.1.144 of Intel Fortran  
 Compiler for Linux  
 Parallel: Yes  
 Firmware: Version 4.0.1 released Oct-2018  
 File System: xfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: Not Applicable  
 Other: None  
 Power Management: --



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Silver 4112  
2.60 GHz)

SPECspeed®2017\_fp\_base = 45.0

SPECspeed®2017\_fp\_peak = Not Run

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Dec-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Oct-2018

## Results Table

Benchmark	Base							Peak						
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
603.bwaves_s	8	<b>260</b>	<b>227</b>	261	226	260	227							
607.cactuBSSN_s	8	367	45.4	367	45.5	<b>367</b>	<b>45.5</b>							
619.lbm_s	8	<b>143</b>	<b>36.6</b>	143	36.6	143	36.6							
621.wrf_s	8	292	45.3	293	45.1	<b>293</b>	<b>45.2</b>							
627.cam4_s	8	<b>409</b>	<b>21.7</b>	409	21.6	408	21.7							
628.pop2_s	8	<b>322</b>	<b>36.9</b>	322	36.9	324	36.7							
638.imagick_s	8	537	26.9	<b>536</b>	<b>26.9</b>	536	26.9							
644.nab_s	8	376	46.5	375	46.5	<b>375</b>	<b>46.5</b>							
649.fotonik3d_s	8	191	47.7	188	48.6	<b>188</b>	<b>48.5</b>							
654.roms_s	8	<b>382</b>	<b>41.2</b>	383	41.1	382	41.2							

SPECspeed®2017\_fp\_base = 45.0

SPECspeed®2017\_fp\_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## General Notes

Environment variables set by runcpu before the start of the run:

KMP\_AFFINITY = "granularity=fine,compact"

LD\_LIBRARY\_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"

OMP\_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM

memory using Redhat Enterprise Linux 7.4

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

## Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Disabled

CPU performance set to Enterprise

(Continued on next page)



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Silver 4112 2.60 GHz)

SPECspeed®2017\_fp\_base = 45.0

SPECspeed®2017\_fp\_peak = Not Run

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Dec-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Oct-2018

### Platform Notes (Continued)

Power Performance Tuning set to OS Controls  
SNC set to Disabled  
Patrol Scrub set to Disabled  
Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f  
running on linux-fdny Mon Dec 10 07:35:45 2018

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

```
From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4112 CPU @ 2.60GHz
 2 "physical id"s (chips)
 8 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 4
  siblings  : 4
  physical 0: cores 0 1 3 4
  physical 1: cores 1 2 4 5
```

```
From lscpu:
Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Byte Order:            Little Endian
CPU(s):                8
On-line CPU(s) list:   0-7
Thread(s) per core:    1
Core(s) per socket:    4
Socket(s):             2
NUMA node(s):         2
Vendor ID:             GenuineIntel
CPU family:            6
Model:                 85
Model name:            Intel(R) Xeon(R) Silver 4112 CPU @ 2.60GHz
Stepping:              4
CPU MHz:               847.858
CPU max MHz:           3000.0000
CPU min MHz:           800.0000
BogoMIPS:              5187.78
Virtualization:        VT-x
L1d cache:             32K
L1i cache:             32K
L2 cache:              1024K
L3 cache:              8448K
NUMA node0 CPU(s):    0-3
```

(Continued on next page)



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Silver 4112  
2.60 GHz)

SPECspeed®2017\_fp\_base = 45.0

SPECspeed®2017\_fp\_peak = Not Run

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Dec-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Oct-2018

### Platform Notes (Continued)

```
NUMA node1 CPU(s):      4-7
Flags:                  fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmpperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 sse3 sdbg
fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts
dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt rsb_ctxsw spec_ctrl stibp
retpoline kaiser tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmil hle
avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt
clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc
```

```
/proc/cpuinfo cache data
cache size : 8448 KB
```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3
node 0 size: 385626 MB
node 0 free: 381620 MB
node 1 cpus: 4 5 6 7
node 1 size: 387054 MB
node 1 free: 383118 MB
node distances:
node  0  1
  0:  10  21
  1:  21  10
```

```
From /proc/meminfo
MemTotal:      791225724 kB
HugePages_Total:      0
Hugepagesize:    2048 kB
```

From /etc/\*release\* /etc/\*version\*

```
SuSE-release:
SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.
os-release:
NAME="SLES"
VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
```

(Continued on next page)



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Silver 4112 2.60 GHz)

SPECspeed®2017\_fp\_base = 45.0

SPECspeed®2017\_fp\_peak = Not Run

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Dec-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Oct-2018

### Platform Notes (Continued)

```
ANSI_COLOR="0;32"  
CPE_NAME="cpe:/o:suse:sles:12:sp2"
```

```
uname -a:  
Linux linux-fdny 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)  
x86_64 x86_64 x86_64 GNU/Linux
```

```
run-level 3 Dec 10 00:53
```

```
SPEC is set to: /home/cpu2017  
Filesystem      Type  Size  Used Avail Use% Mounted on  
/dev/sda2       xfs   500G  168G  333G  34% /
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.4.0.1.139.1003182220 10/03/2018

Memory:

24x 0xCE00 M393A4K40CB2-CTD 32 GB 2 rank 2666, configured at 2400

(End of data from sysinfo program)

### Compiler Version Notes

```
=====  
C | 619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)  
=====
```

```
icc (ICC) 19.0.1.144 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
=====
```

```
=====  
C++, C, Fortran | 607.cactuBSSN_s(base)  
=====
```

```
icpc (ICC) 19.0.1.144 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
icc (ICC) 19.0.1.144 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
ifort (IFORT) 19.0.1.144 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
=====
```

```
=====  
Fortran | 603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)  
=====
```

(Continued on next page)



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Silver 4112  
2.60 GHz)

SPECspeed®2017\_fp\_base = 45.0

SPECspeed®2017\_fp\_peak = Not Run

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Dec-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Oct-2018

### Compiler Version Notes (Continued)

ifort (IFORT) 19.0.1.144 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

-----  
=====  
Fortran, C | 621.wrf\_s(base) 627.cam4\_s(base) 628.pop2\_s(base)

-----  
ifort (IFORT) 19.0.1.144 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
icc (ICC) 19.0.1.144 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
-----

### Base Compiler Invocation

C benchmarks:

```
icc -m64 -std=c11
```

Fortran benchmarks:

```
ifort -m64
```

Benchmarks using both Fortran and C:

```
ifort -m64 icc -m64 -std=c11
```

Benchmarks using Fortran, C, and C++:

```
icpc -m64 icc -m64 -std=c11 ifort -m64
```

### Base Portability Flags

```
603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64
```



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Silver 4112  
2.60 GHz)

SPECspeed®2017\_fp\_base = 45.0

SPECspeed®2017\_fp\_peak = Not Run

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Dec-2018

**Hardware Availability:** Aug-2017

**Software Availability:** Oct-2018

## Base Optimization Flags

### C benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
```

### Fortran benchmarks:

```
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp  
-nostandard-realloc-lhs -align array32byte
```

### Benchmarks using both Fortran and C:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP  
-nostandard-realloc-lhs -align array32byte
```

### Benchmarks using Fortran, C, and C++:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP  
-nostandard-realloc-lhs -align array32byte
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml>

SPEC CPU and SPECspeed are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact [info@spec.org](mailto:info@spec.org).

Tested with SPEC CPU®2017 v1.0.2 on 2018-12-10 10:35:44-0500.

Report generated on 2020-09-04 14:37:01 by CPU2017 PDF formatter v6255.

Originally published on 2019-01-29.