



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6150, 2.70 GHz)

SPECspeed®2017\_fp\_base = 178

SPECspeed®2017\_fp\_peak = Not Run

CPU2017 License: 9019

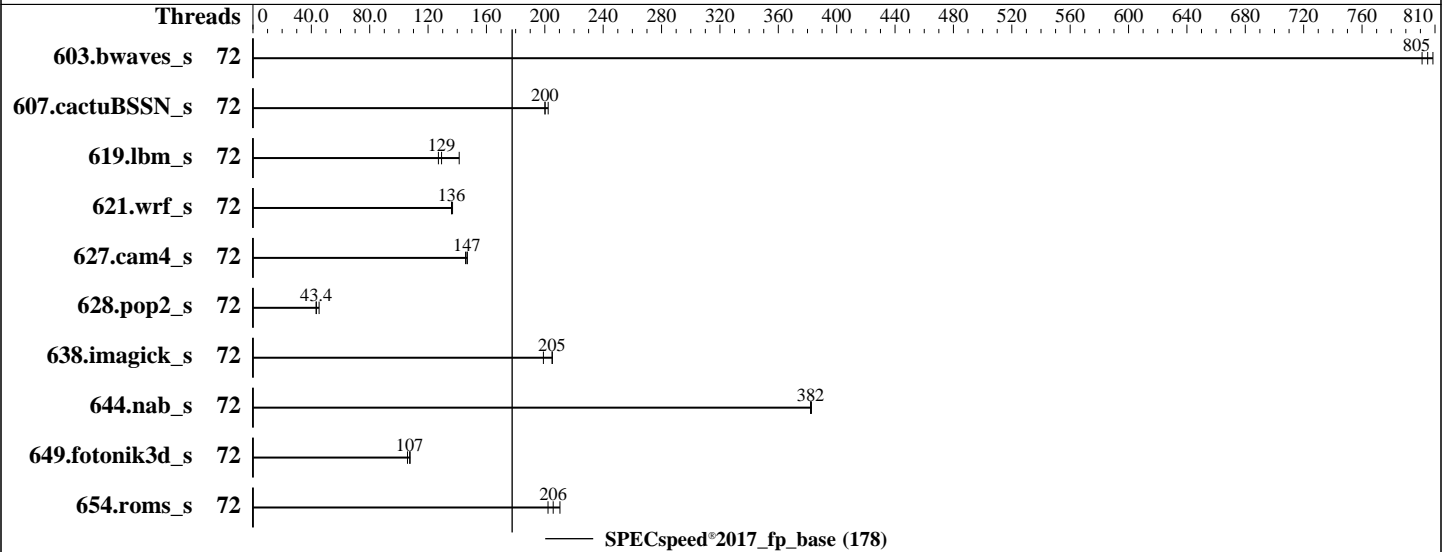
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jan-2019

Hardware Availability: Aug-2017

Software Availability: Oct-2018



### Hardware

CPU Name: Intel Xeon Gold 6150  
 Max MHz: 3700  
 Nominal: 2700  
 Enabled: 72 cores, 4 chips  
 Orderable: 2,4 Chips  
 Cache L1: 32 KB I + 32 KB D on chip per core  
 L2: 1 MB I+D on chip per core  
 L3: 24.75 MB I+D on chip per chip  
 Other: None  
 Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2666V-R)  
 Storage: 1 x 1 TB HDD, 7.2K RPM  
 Other: None

### Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86\_64) 4.4.120-92.70-default  
 Compiler: C/C++: Version 19.0.0.117 of Intel C/C++ Compiler for Linux;  
 Fortran: Version 19.0.0.117 of Intel Fortran Compiler for Linux  
 Parallel: Yes  
 Firmware: Version 3.1.3e released Jun-2018  
 File System: xfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: Not Applicable  
 Other: None  
 Power Management: --



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6150, 2.70 GHz)

SPECspeed®2017\_fp\_base = 178

SPECspeed®2017\_fp\_peak = Not Run

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Jan-2019  
**Hardware Availability:** Aug-2017  
**Software Availability:** Oct-2018

## Results Table

Benchmark	Base							Peak						
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
603.bwaves_s	72	<b><u>73.3</u></b>	<b><u>805</u></b>	73.6	801	73.0	809							
607.cactuBSSN_s	72	82.4	202	83.3	200	<b><u>83.3</u></b>	<b><u>200</u></b>							
619.lbm_s	72	41.2	127	37.1	141	<b><u>40.5</u></b>	<b><u>129</u></b>							
621.wrf_s	72	<b><u>97.2</u></b>	<b><u>136</u></b>	97.2	136	96.7	137							
627.cam4_s	72	60.8	146	60.3	147	<b><u>60.4</u></b>	<b><u>147</u></b>							
628.pop2_s	72	262	45.3	274	43.3	<b><u>273</u></b>	<b><u>43.4</u></b>							
638.imagick_s	72	72.5	199	<b><u>70.4</u></b>	<b><u>205</u></b>	70.3	205							
644.nab_s	72	45.7	382	45.7	383	<b><u>45.7</u></b>	<b><u>382</u></b>							
649.fotonik3d_s	72	86.1	106	<b><u>84.9</u></b>	<b><u>107</u></b>	84.6	108							
654.roms_s	72	74.8	210	77.9	202	<b><u>76.5</u></b>	<b><u>206</u></b>							

SPECspeed®2017\_fp\_base = 178

SPECspeed®2017\_fp\_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## General Notes

Environment variables set by runcpu before the start of the run:

KMP\_AFFINITY = "granularity=fine,compact"

LD\_LIBRARY\_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"

OMP\_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM

memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

## Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Disabled

CPU performance set to Enterprise

(Continued on next page)



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6150, 2.70 GHz)

SPECspeed®2017\_fp\_base = 178

SPECspeed®2017\_fp\_peak = Not Run

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Jan-2019

**Hardware Availability:** Aug-2017

**Software Availability:** Oct-2018

### Platform Notes (Continued)

Power Performance Tuning set to OS Controls  
 SNC set to Disabled  
 Patrol Scrub set to Disabled  
 Sysinfo program /home/cpu2017/bin/sysinfo  
 Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9  
 running on linux-9r4j Sat Jan 5 01:35:52 2019

SUT (System Under Test) info as seen by some common utilities.  
 For more information on this section, see  
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

```
From /proc/cpuinfo
model name      : Intel(R) Xeon(R) Gold 6150 CPU @ 2.70GHz
 4 "physical id"s (chips)
 72 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores      : 18
siblings       : 18
physical 0:    cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 1:    cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 2:    cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 3:    cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
```

```
From lscpu:
Architecture:      x86_64
CPU op-mode(s):    32-bit, 64-bit
Byte Order:        Little Endian
CPU(s):            72
On-line CPU(s) list: 0-71
Thread(s) per core: 1
Core(s) per socket: 18
Socket(s):         4
NUMA node(s):     4
Vendor ID:        GenuineIntel
CPU family:        6
Model:            85
Model name:        Intel(R) Xeon(R) Gold 6150 CPU @ 2.70GHz
Stepping:         4
CPU MHz:          1536.561
CPU max MHz:      3700.0000
CPU min MHz:      1200.0000
BogoMIPS:         5394.19
Virtualization:    VT-x
L1d cache:        32K
L1i cache:        32K
L2 cache:         1024K
```

(Continued on next page)



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6150, 2.70 GHz)

SPECspeed®2017\_fp\_base = 178

SPECspeed®2017\_fp\_peak = Not Run

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Jan-2019

**Hardware Availability:** Aug-2017

**Software Availability:** Oct-2018

### Platform Notes (Continued)

L3 cache: 25344K  
NUMA node0 CPU(s): 0-17  
NUMA node1 CPU(s): 18-35  
NUMA node2 CPU(s): 36-53  
NUMA node3 CPU(s): 54-71

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant\_tsc art arch\_perfmon pebs bts rep\_good nopl xtopology nonstop\_tsc aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds\_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4\_1 sse4\_2 x2apic movbe popcnt tsc\_deadline\_timer aes xsave avx f16c rdrand lahf\_lm abm 3dnowprefetch ida arat epb invpcid\_single pln pts dtherm hwp hwp\_act\_window hwp\_epp hwp\_pkg\_req intel\_pt rsb\_ctxsw spec\_ctrl stibp retpoline kaiser tpr\_shadow vnmi flexpriority ept vpid fsgsbase tsc\_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm\_llc cqm\_occup\_llc

```
/proc/cpuinfo cache data
cache size : 25344 KB
```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
node 0 size: 385622 MB
node 0 free: 382339 MB
node 1 cpus: 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35
node 1 size: 387057 MB
node 1 free: 384223 MB
node 2 cpus: 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53
node 2 size: 387057 MB
node 2 free: 382337 MB
node 3 cpus: 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71
node 3 size: 387054 MB
node 3 free: 381446 MB
node distances:
node  0  1  2  3
 0:  10  21  21  21
 1:  21  10  21  21
 2:  21  21  10  21
 3:  21  21  21  10
```

```
From /proc/meminfo
MemTotal: 1583914480 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
```

```
From /etc/*release* /etc/*version*
```

(Continued on next page)



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6150, 2.70 GHz)

SPECspeed®2017\_fp\_base = 178

SPECspeed®2017\_fp\_peak = Not Run

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Jan-2019  
**Hardware Availability:** Aug-2017  
**Software Availability:** Oct-2018

### Platform Notes (Continued)

```

SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 2
  # This file is deprecated and will be removed in a future service pack or release.
  # Please check /etc/os-release for details about this release.
os-release:
  NAME="SLES"
  VERSION="12-SP2"
  VERSION_ID="12.2"
  PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
  ID="sles"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:12:sp2"

```

```

uname -a:
Linux linux-9r4j 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
x86_64 x86_64 x86_64 GNU/Linux

```

Kernel self-reported vulnerability status:

```

CVE-2017-5754 (Meltdown):           Mitigation: PTI
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: IBRS+IBPB

```

```
run-level 3 Nov 26 08:51
```

```

SPEC is set to: /home/cpu2017
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sda1       xfs   930G   48G  883G   6% /

```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C480M5.3.1.3e.0.0613181101 06/13/2018

```

Memory:
48x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666

```

(End of data from sysinfo program)

### Compiler Version Notes

```

=====
C | 619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)
=====

```

(Continued on next page)



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6150, 2.70 GHz)

SPECspeed®2017\_fp\_base = 178

SPECspeed®2017\_fp\_peak = Not Run

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Jan-2019  
**Hardware Availability:** Aug-2017  
**Software Availability:** Oct-2018

### Compiler Version Notes (Continued)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.0.117 Build 20180804  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====  
C++, C, Fortran | 607.cactuBSSN\_s(base)

=====  
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.0.117 Build 20180804  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.0.117 Build 20180804  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.0.117 Build 20180804  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====  
Fortran | 603.bwaves\_s(base) 649.fotonik3d\_s(base) 654.roms\_s(base)

=====  
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.0.117 Build 20180804  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====  
Fortran, C | 621.wrf\_s(base) 627.cam4\_s(base) 628.pop2\_s(base)

=====  
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.0.117 Build 20180804  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.0.117 Build 20180804  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

### Base Compiler Invocation

C benchmarks:  
icc -m64 -std=c11

Fortran benchmarks:  
ifort -m64

(Continued on next page)



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6150, 2.70 GHz)

SPECspeed®2017\_fp\_base = 178

SPECspeed®2017\_fp\_peak = Not Run

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Jan-2019

**Hardware Availability:** Aug-2017

**Software Availability:** Oct-2018

## Base Compiler Invocation (Continued)

Benchmarks using both Fortran and C:

```
ifort -m64 icc -m64 -std=c11
```

Benchmarks using Fortran, C, and C++:

```
icpc -m64 icc -m64 -std=c11 ifort -m64
```

## Base Portability Flags

```
603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64
```

## Base Optimization Flags

C benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
```

Fortran benchmarks:

```
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-nostandard-realloc-lhs -align array32byte
```

Benchmarks using both Fortran and C:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte
```

Benchmarks using Fortran, C, and C++:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte
```



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6150, 2.70 GHz)

SPECspeed®2017\_fp\_base = 178

SPECspeed®2017\_fp\_peak = Not Run

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Jan-2019

**Hardware Availability:** Aug-2017

**Software Availability:** Oct-2018

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml>

SPEC CPU and SPECspeed are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact [info@spec.org](mailto:info@spec.org).

Tested with SPEC CPU®2017 v1.0.5 on 2019-01-05 01:35:52-0500.

Report generated on 2020-07-01 12:59:53 by CPU2017 PDF formatter v6255.

Originally published on 2019-01-29.