SPEC® CINT2006 Result

Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Platinum 8176M, 2.10 GHz)

SPECint®_rate2006 = 2620

SPECint_rate_base2006 = 2520

CPU2006 license: 9019	**Test date:** Nov-2017
Test sponsor: Cisco Systems	**Hardware Availability:** Aug-2017
Tested by: Cisco Systems	**Software Availability:** Apr-2017

Copies

Benchmark	112 (peak)	112 (base)
400.perlbench	2310	1920
401.bzip2	1210	1160
403.gcc	1750	1720
429.mcf		3180
445.gobmk	1670	1670
456.hmmer	3770	3360
458.sjeng	1850	1750
462.libquantum		45300
464.h264ref	3100	2960
471.omnetpp	1230	1180
473.astar		1320
483.xalancbmk		2570

SPECint_rate_base2006 = 2520

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Hardware

CPU Name:	Intel Xeon Platinum 8176M
CPU Characteristics:	Intel Turbo Boost Technology up to 3.80 GHz
CPU MHz:	2100
FPU:	Integrated
CPU(s) enabled:	56 cores, 2 chips, 28 cores/chip, 2 threads/core
CPU(s) orderable:	1,2 chips
Primary Cache:	32 KB I + 32 KB D on chip per core
Secondary Cache:	1 MB I+D on chip per core
L3 Cache:	38.5 MB I+D on chip per chip
Other Cache:	None
Memory:	384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)
Disk Subsystem:	1 x 600 GB SAS HDD, 10K RPM
Other Hardware:	None

Software

Operating System:	SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default
Compiler:	C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux; Fortran: Version 18.0.0.128 of Intel Fortran
Auto Parallel:	Yes
File System:	xfs
System State:	Run level 3 (multi-user)
Base Pointers:	32-bit
Peak Pointers:	32/64-bit
Other Software:	Microquill SmartHeap V10.2

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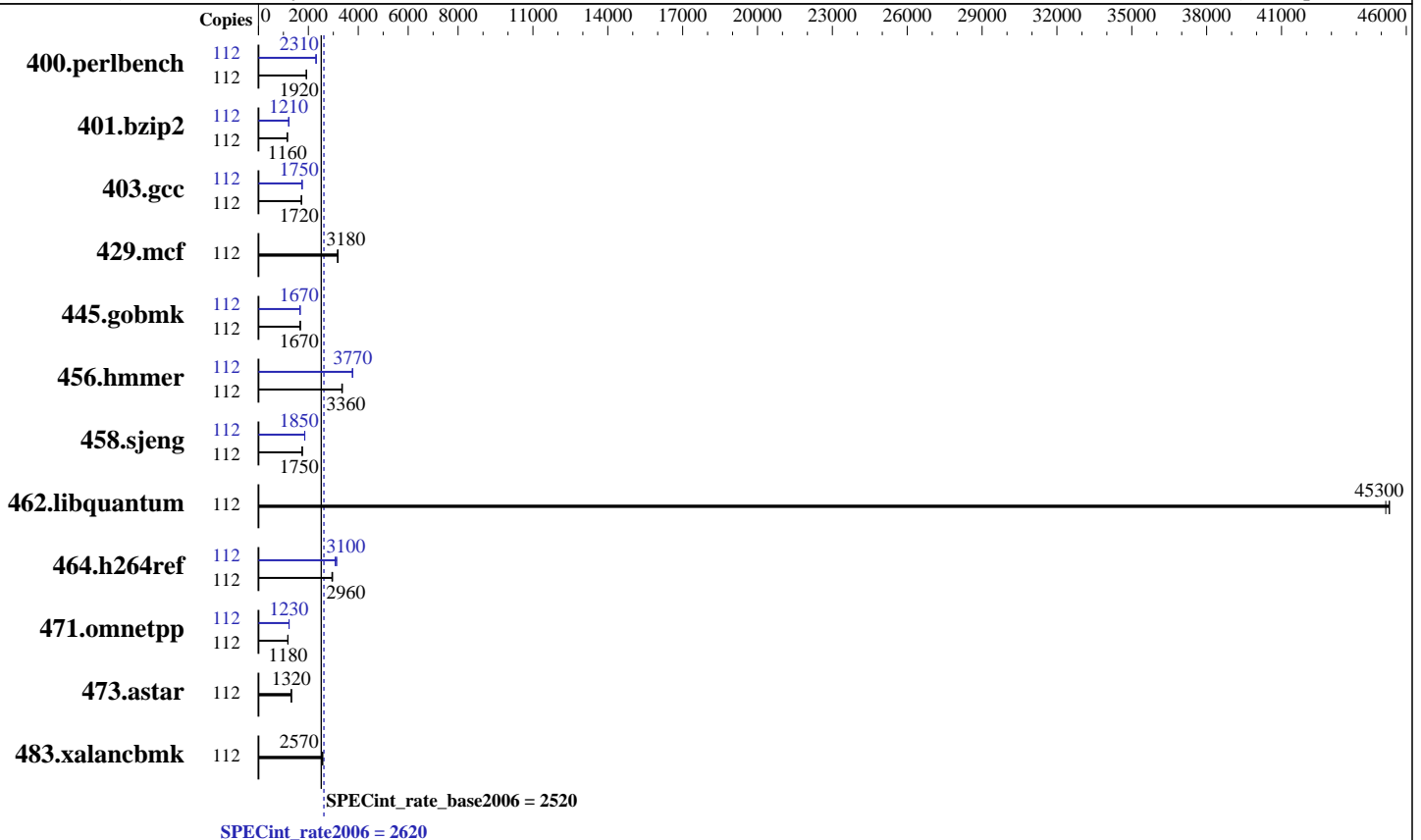
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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	112	**569**	**1920**	569	1920	570	1920	112	**474**	**2310**	473	2310	475	2310
401.bzip2	112	933	1160	936	1160	**933**	**1160**	112	**890**	**1210**	890	1210	889	1220
403.gcc	112	524	1720	**524**	**1720**	523	1720	112	**516**	**1750**	516	1750	514	1750
429.mcf	112	320	3190	322	3170	**322**	**3180**	112	320	3190	322	3170	**322**	**3180**
445.gobmk	112	**702**	**1670**	702	1670	701	1680	112	707	1660	**704**	**1670**	703	1670
456.hmmer	112	313	3340	**311**	**3360**	311	3360	112	278	3760	276	3780	**277**	**3770**
458.sjeng	112	**773**	**1750**	773	1750	773	1750	112	**732**	**1850**	732	1850	730	1860
462.libquantum	112	51.2	45300	**51.2**	**45300**	51.4	45200	112	51.2	45300	**51.2**	**45300**	51.4	45200
464.h264ref	112	**837**	**2960**	842	2940	835	2970	112	**799**	**3100**	790	3140	806	3080
471.omnetpp	112	594	1180	**593**	**1180**	592	1180	112	**571**	**1230**	571	1220	571	1230
473.astar	112	**596**	**1320**	597	1320	596	1320	112	**596**	**1320**	597	1320	596	1320
483.xalancbmk	112	300	2580	**301**	**2570**	301	2570	112	300	2580	**301**	**2570**	301	2570

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

   The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

   Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

    BIOS Settings:
    Intel HyperThreading Technology set to Enabled
    CPU performance set to Enterprise
    Power Performance Tuning set to OS
    SNC set to Enabled
    IMC Interleaving set to 1-way Interleave
    Patrol Scrub set to Disabled
     Sysinfo program /home/cpu2006-1.2/config/sysinfo.rev6993
     Revision 6993 of 2015-11-06 (b5e8d4b4eb51ed28d7f98696cbe290c1)
     running on linux-3joc Fri Nov 17 20:10:00 2017

     This section contains SUT (System Under Test) info as seen by
     some common utilities. To remove or add to this section, see:
       http://www.spec.org/cpu2006/Docs/config.html#sysinfo

     From /proc/cpuinfo
        model name : Intel(R) Xeon(R) Platinum 8176M CPU @ 2.10GHz
                        Continued on next page

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Platform Notes (Continued)

```
     2 "physical id"s (chips)
     112 "processors"
  cores, siblings (Caution: counting these is hw and system dependent.  The
  following excerpts from /proc/cpuinfo might not be reliable.  Use with
  caution.)
     cpu cores : 28
     siblings  : 56
     physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24
     25 26 27 28 29 30
     physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24
     25 26 27 28 29 30
  cache size : 39424 KB

From /proc/meminfo
  MemTotal:       394863904 kB
  HugePages_Total:        0
  Hugepagesize:        2048 kB

/usr/bin/lsb_release -d
  SUSE Linux Enterprise Server 12 SP2

From /etc/*release* /etc/*version*
  SuSE-release:
     SUSE Linux Enterprise Server 12 (x86_64)
     VERSION = 12
     PATCHLEVEL = 2
     # This file is deprecated and will be removed in a future service pack or
     release.
     # Please check /etc/os-release for details about this release.
  os-release:
     NAME="SLES"
     VERSION="12-SP2"
     VERSION_ID="12.2"
     PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
     ID="sles"
     ANSI_COLOR="0;32"
     CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
  Linux linux-3joc 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016
  (9464f67) x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Nov 17 19:44

SPEC is set to: /home/cpu2006-1.2
  Filesystem      Type  Size  Used Avail Use% Mounted on
  /dev/sda3       xfs   516G  112G  404G  22% /home
Additional information from dmidecode:

  Warning: Use caution when you interpret this section. The 'dmidecode' program
  reads system data which is "intended to allow hardware to be accurately
  determined", but the intent may not be met, as there are frequent changes to
```

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Platform Notes (Continued)

```
   hardware, firmware, and the "DMTF SMBIOS" standard.

  BIOS Cisco Systems, Inc. C220M5.3.1.1d.0.0615170645 06/15/2017
  Memory:
   24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz

 (End of data from sysinfo program)
```

General Notes

```
Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/intel/lib/ia32:/opt/intel/lib/intel64:/home/cpu2006-1.2/sh10.2"

 Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
 memory using Redhat Enterprise Linux 7.2
 Transparent Huge Pages enabled with:
 echo always > /sys/kernel/mm/transparent_hugepage/enabled
 Filesystem page cache cleared with:
 shell invocation of 'sync; echo 3 > /proc/sys/vm/drop_caches' prior to run
 runspec command invoked through numactl i.e.:
 numactl --interleave=all runspec <etc>
```

Base Compiler Invocation

C benchmarks:
```
     icc -m32 -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
```

C++ benchmarks:
```
     icpc -m32 -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
```

Base Portability Flags

```
  400.perlbench: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX_IA32
     401.bzip2: -D_FILE_OFFSET_BITS=64
      403.gcc: -D_FILE_OFFSET_BITS=64
      429.mcf: -D_FILE_OFFSET_BITS=64
     445.gobmk: -D_FILE_OFFSET_BITS=64
     456.hmmer: -D_FILE_OFFSET_BITS=64
     458.sjeng: -D_FILE_OFFSET_BITS=64
   462.libquantum: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
    464.h264ref: -D_FILE_OFFSET_BITS=64
    471.omnetpp: -D_FILE_OFFSET_BITS=64
     473.astar: -D_FILE_OFFSET_BITS=64
   483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
```

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Base Optimization Flags

C benchmarks:
```
-xHOST -ipo -O3 -no-prec-div -qopt-prefetch -qopt-mem-layout-trans=3
```

C++ benchmarks:
```
-xHOST -ipo -O3 -no-prec-div -qopt-prefetch -qopt-mem-layout-trans=3
-Wl,-z,muldefs -L/home/cpu2006-1.2/sh10.2 -lsmartheap
```

Base Other Flags

C benchmarks:

> 403.gcc: `-Dalloca=_alloca`

Peak Compiler Invocation

C benchmarks (except as noted below):
```
icc -m32 -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
```

> 400.perlbench: `icc -m64`

> 401.bzip2: `icc -m64`

> 456.hmmer: `icc -m64`

> 458.sjeng: `icc -m64`

C++ benchmarks:
```
icpc -m32 -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
```

Peak Portability Flags

> 400.perlbench: `-DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64`
> 401.bzip2: `-DSPEC_CPU_LP64`
> 403.gcc: `-D_FILE_OFFSET_BITS=64`
> 429.mcf: `-D_FILE_OFFSET_BITS=64`
> 445.gobmk: `-D_FILE_OFFSET_BITS=64`
> 456.hmmer: `-DSPEC_CPU_LP64`
> 458.sjeng: `-DSPEC_CPU_LP64`
> 462.libquantum: `-D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX`
> 464.h264ref: `-D_FILE_OFFSET_BITS=64`
> 471.omnetpp: `-D_FILE_OFFSET_BITS=64`
> 473.astar: `-D_FILE_OFFSET_BITS=64`
> 483.xalancbmk: `-D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX`

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Peak Optimization Flags

C benchmarks:

    400.perlbench: `-prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)`
`-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)`
`-no-prec-div(pass 2) -auto-ilp32 -qopt-mem-layout-trans=3`

    401.bzip2: `-prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)`
`-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)`
`-no-prec-div(pass 2) -qopt-prefetch -auto-ilp32`
`-qopt-mem-layout-trans=3`

    403.gcc: `-xHOST -ipo -O3 -no-prec-div -qopt-mem-layout-trans=3`

    429.mcf: `basepeak = yes`

    445.gobmk: `-prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)`
`-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)`
`-no-prec-div(pass 2) -qopt-mem-layout-trans=3`

    456.hmmer: `-xHOST -ipo -O3 -no-prec-div -unroll2 -auto-ilp32`
`-qopt-mem-layout-trans=3`

    458.sjeng: `-prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)`
`-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)`
`-no-prec-div(pass 2) -unroll4 -auto-ilp32`
`-qopt-mem-layout-trans=3`

    462.libquantum: `basepeak = yes`

    464.h264ref: `-prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)`
`-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)`
`-no-prec-div(pass 2) -unroll2 -qopt-mem-layout-trans=3`

C++ benchmarks:

    471.omnetpp: `-prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)`
`-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)`
`-no-prec-div(pass 2)`
`-qopt-ra-region-strategy=block`
`-qopt-mem-layout-trans=3 -Wl,-z,muldefs`
`-L/home/cpu2006-1.2/sh10.2 -lsmartheap`

    473.astar: `basepeak = yes`

    483.xalancbmk: `basepeak = yes`

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Peak Other Flags

C benchmarks:

403.gcc: `-Dalloca=_alloca`

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.xml

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

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