SPEC® CINT2006 Result

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8176 2.10GHz)

SPECint®_rate2006 = 4950

SPECint_rate_base2006 = 4730

CPU2006 license: 9019
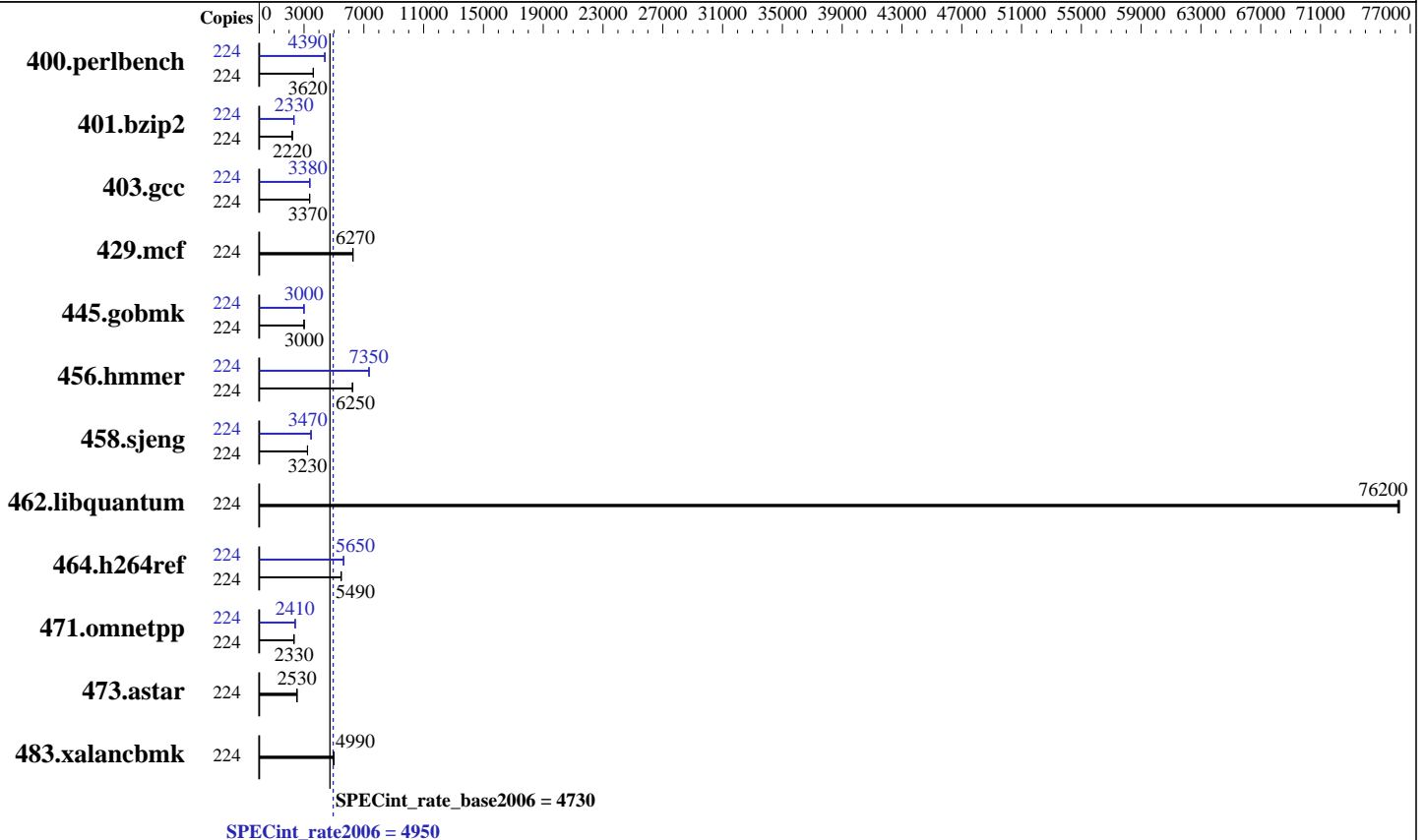
Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Aug-2017

Hardware Availability: Aug-2017

Software Availability: Apr-2017

SPECint_rate_base2006 = 4730

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Hardware

CPU Name:	Intel Xeon Platinum 8176
CPU Characteristics:	Intel Turbo Boost Technology up to 3.80 GHz
CPU MHz:	2100
FPU:	Integrated
CPU(s) enabled:	112 cores, 4 chips, 28 cores/chip, 2 threads/core
CPU(s) orderable:	2,4 chips
Primary Cache:	32 KB I + 32 KB D on chip per core
Secondary Cache:	1 MB I+D on chip per core
L3 Cache:	38.5 MB I+D on chip per chip
Other Cache:	None
Memory:	768 GB (48 x 16 GB 2Rx4 PC4-2666V-R)
Disk Subsystem:	1 x 800 GB SAS SSD
Other Hardware:	None

Software

Operating System:	SUSE Linux Enterprise Server 12 SP2 4.4.21-69-default
Compiler:	C/C++: Version 17.0.3.191 of Intel C/C++ Compiler for Linux
Auto Parallel:	Yes
File System:	xfs
System State:	Run level 5 (multi-user)
Base Pointers:	32-bit
Peak Pointers:	32/64-bit
Other Software:	Microquill SmartHeap V10.2

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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	224	604	3620	605	3610	**604**	**3620**	224	**498**	**4390**	498	4400	499	4380
401.bzip2	224	981	2200	974	2220	**974**	**2220**	224	934	2310	**929**	**2330**	928	2330
403.gcc	224	534	3380	535	3370	**534**	**3370**	224	532	3390	**533**	**3380**	533	3380
429.mcf	224	326	6280	**326**	**6270**	326	6260	224	326	6280	**326**	**6270**	326	6260
445.gobmk	224	781	3010	**782**	**3000**	783	3000	224	785	2990	783	3000	**784**	**3000**
456.hmmer	224	336	6230	**335**	**6250**	334	6260	224	284	7350	284	7350	**284**	**7350**
458.sjeng	224	838	3230	840	3230	**839**	**3230**	224	**781**	**3470**	782	3470	780	3470
462.libquantum	224	60.9	76200	**60.9**	**76200**	60.8	76300	224	60.9	76200	**60.9**	**76200**	60.8	76300
464.h264ref	224	906	5470	**903**	**5490**	902	5490	224	877	5650	**878**	**5650**	879	5640
471.omnetpp	224	602	2320	601	2330	**601**	**2330**	224	**582**	**2410**	580	2410	582	2410
473.astar	224	**622**	**2530**	622	2530	622	2530	224	**622**	**2530**	622	2530	622	2530
483.xalancbmk	224	311	4960	**309**	**4990**	309	5000	224	311	4960	**309**	**4990**	309	5000

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

    The numactl mechanism was used to bind copies to processors. The config file option 'submit'
    was used to generate numactl commands to bind each copy to a specific processor.
    For details, please see the config file.

Operating System Notes

    Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

    BIOS Settings:
    Intel HyperThreading Technology set to Enabled
    CPU performance set to Enterprise
    Power Performance Tuning set to OS
    SNC set to Enabled
    IMC Interleaving set to 1-way Interleave
    Patrol Scrub set to Disabled
     Sysinfo program /home/cpu2006-1.2/config/sysinfo.rev6993
     Revision 6993 of 2015-11-06 (b5e8d4b4eb51ed28d7f98696cbe290c1)
     running on linux-g4f1 Thu Aug 10 22:55:49 2017

     This section contains SUT (System Under Test) info as seen by
     some common utilities. To remove or add to this section, see:
       http://www.spec.org/cpu2006/Docs/config.html#sysinfo

     From /proc/cpuinfo
        model name : Intel(R) Xeon(R) Platinum 8176 CPU @ 2.10GHz

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Platform Notes (Continued)

```
     4 "physical id"s (chips)
     224 "processors"
  cores, siblings (Caution: counting these is hw and system dependent.  The
  following excerpts from /proc/cpuinfo might not be reliable.  Use with
  caution.)
     cpu cores : 28
     siblings  : 56
     physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24
     25 26 27 28 29 30
     physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24
     25 26 27 28 29 30
     physical 2: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24
     25 26 27 28 29 30
     physical 3: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24
     25 26 27 28 29 30
  cache size : 39424 KB

From /proc/meminfo
   MemTotal:       790966816 kB
   HugePages_Total:        0
   Hugepagesize:        2048 kB

/usr/bin/lsb_release -d
   SUSE Linux Enterprise Server 12 SP2

From /etc/*release* /etc/*version*
   SuSE-release:
     SUSE Linux Enterprise Server 12 (x86_64)
     VERSION = 12
     PATCHLEVEL = 2
     # This file is deprecated and will be removed in a future service pack or
     release.
     # Please check /etc/os-release for details about this release.
   os-release:
     NAME="SLES"
     VERSION="12-SP2"
     VERSION_ID="12.2"
     PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
     ID="sles"
     ANSI_COLOR="0;32"
     CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
   Linux linux-g4f1 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016
   (9464f67) x86_64 x86_64 x86_64 GNU/Linux

run-level 5 Aug 9 22:12

SPEC is set to: /home/cpu2006-1.2
   Filesystem      Type  Size  Used Avail Use% Mounted on
   /dev/sda6       xfs   871G   34G  837G   4% /home
Additional information from dmidecode:
```
Continued on next page

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Platform Notes (Continued)

```
   Warning: Use caution when you interpret this section. The 'dmidecode' program
   reads system data which is "intended to allow hardware to be accurately
   determined", but the intent may not be met, as there are frequent changes to
   hardware, firmware, and the "DMTF SMBIOS" standard.

  BIOS Cisco Systems, Inc. C480M5.3.1.0.248.0518171057 05/18/2017
  Memory:
   48x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz

 (End of data from sysinfo program)
```

General Notes

```
Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2006-1.2/lib/ia32:/home/cpu2006-1.2/lib/intel64:/home/cpu2006-1.2/sh10.2"

 Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
 memory using Redhat Enterprise Linux 7.2
 Transparent Huge Pages enabled with:
 echo always > /sys/kernel/mm/transparent_hugepage/enabled
 Filesystem page cache cleared with:
 shell invocation of 'sync; echo 3 > /proc/sys/vm/drop_caches' prior to run
 runspec command invoked through numactl i.e.:
 numactl --interleave=all runspec <etc>
```

Base Compiler Invocation

C benchmarks:

```
    icc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32
```

C++ benchmarks:

```
    icpc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32
```

Base Portability Flags

```
    400.perlbench: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX_IA32
      401.bzip2: -D_FILE_OFFSET_BITS=64
        403.gcc: -D_FILE_OFFSET_BITS=64
        429.mcf: -D_FILE_OFFSET_BITS=64
      445.gobmk: -D_FILE_OFFSET_BITS=64
      456.hmmer: -D_FILE_OFFSET_BITS=64
      458.sjeng: -D_FILE_OFFSET_BITS=64
    462.libquantum: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
      464.h264ref: -D_FILE_OFFSET_BITS=64
      471.omnetpp: -D_FILE_OFFSET_BITS=64
```

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Base Portability Flags (Continued)

473.astar: `-D_FILE_OFFSET_BITS=64`
483.xalancbmk: `-D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX`

Base Optimization Flags

C benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-qopt-mem-layout-trans=3
```

C++ benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-qopt-mem-layout-trans=3 -Wl,-z,muldefs -L/sh10.2 -lsmartheap
```

Base Other Flags

C benchmarks:

403.gcc: `-Dalloca=_alloca`

Peak Compiler Invocation

C benchmarks (except as noted below):
`icc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32`

400.perlbench: `icc -m64`

401.bzip2: `icc -m64`

456.hmmer: `icc -m64`

458.sjeng: `icc -m64`

C++ benchmarks:
`icpc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32`

Peak Portability Flags

400.perlbench: `-DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64`
401.bzip2: `-DSPEC_CPU_LP64`
403.gcc: `-D_FILE_OFFSET_BITS=64`
429.mcf: `-D_FILE_OFFSET_BITS=64`

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Peak Portability Flags (Continued)

```
    445.gobmk: -D_FILE_OFFSET_BITS=64
    456.hmmer: -DSPEC_CPU_LP64
    458.sjeng: -DSPEC_CPU_LP64
 462.libquantum: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
   464.h264ref: -D_FILE_OFFSET_BITS=64
   471.omnetpp: -D_FILE_OFFSET_BITS=64
     473.astar: -D_FILE_OFFSET_BITS=64
 483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
```

Peak Optimization Flags

C benchmarks:

```
  400.perlbench: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512(pass 2)
                 -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
                 -no-prec-div(pass 2) -auto-ilp32 -qopt-mem-layout-trans=3

     401.bzip2: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512(pass 2)
                 -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
                 -no-prec-div(pass 2) -qopt-prefetch -auto-ilp32
                 -qopt-mem-layout-trans=3

       403.gcc: -xCORE-AVX512 -ipo -O3 -no-prec-div
                 -qopt-mem-layout-trans=3

       429.mcf: basepeak = yes

    445.gobmk: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512(pass 2)
                 -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
                 -no-prec-div(pass 2) -qopt-mem-layout-trans=3

    456.hmmer: -xCORE-AVX512 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32
                 -qopt-mem-layout-trans=3

    458.sjeng: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512(pass 2)
                 -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
                 -no-prec-div(pass 2) -unroll4 -auto-ilp32
                 -qopt-mem-layout-trans=3

 462.libquantum: basepeak = yes

   464.h264ref: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512(pass 2)
                 -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
                 -no-prec-div(pass 2) -unroll2 -qopt-mem-layout-trans=3
```

C++ benchmarks:

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Peak Optimization Flags (Continued)

471.omnetpp: `-prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512(pass 2)`
`-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)`
`-no-prec-div(pass 2)`
`-qopt-ra-region-strategy=block`
`-qopt-mem-layout-trans=3 -Wl,-z,muldefs`
`-L/sh10.2 -lsmartheap`

473.astar: `basepeak = yes`

483.xalancbmk: `basepeak = yes`

Peak Other Flags

C benchmarks:

403.gcc: `-Dalloca=_alloca`

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.xml

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

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