



SPEC® CINT2006 Result

Copyright 2006-2015 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B420 M4 (Intel Xeon E5-4650 v3, 2.10 GHz)

SPECint®2006 = 52.7

SPECint_base2006 = 51.1

CPU2006 license: 9019

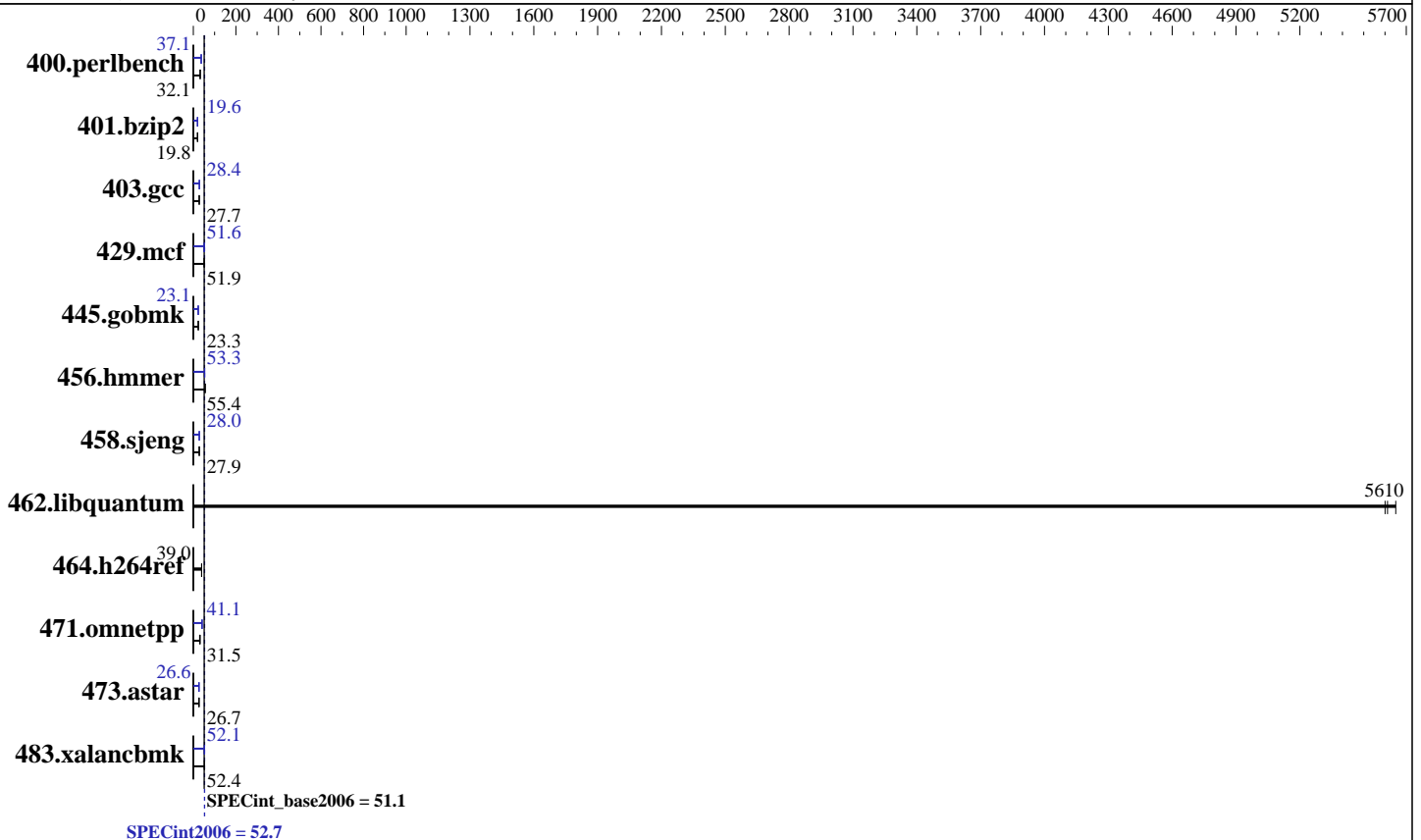
Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Aug-2015

Hardware Availability: Jun-2015

Software Availability: Nov-2014



Hardware

CPU Name: Intel Xeon E5-4650 v3
CPU Characteristics: Intel Turbo Boost Technology up to 2.80 GHz
CPU MHz: 2100
FPU: Integrated
CPU(s) enabled: 48 cores, 4 chips, 12 cores/chip
CPU(s) orderable: 2,4 chip
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 256 KB I+D on chip per core
L3 Cache: 30 MB I+D on chip per chip
Other Cache: None
Memory: 512 GB (32 x 16 GB 2Rx4 PC4-2133P-R)
Disk Subsystem: 1 x 300 GB SAS, 15K RPM
Other Hardware: None

Software

Operating System: SUSE Linux Enterprise Server 12 (x86_64)
 3.12.28-4-default
Compiler: C/C++: Version 15.0.0.090 of Intel C++ Studio XE for Linux
Auto Parallel: Yes
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 32/64-bit
Peak Pointers: 32/64-bit
Other Software: Microquill SmartHeap V10.0



SPEC CINT2006 Result

Copyright 2006-2015 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B420 M4 (Intel Xeon E5-4650 v3, 2.10 GHz)

SPECint2006 = **52.7**

SPECint_base2006 = **51.1**

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Aug-2015
Hardware Availability: Jun-2015
Software Availability: Nov-2014

Results Table

Benchmark	Base						Peak					
	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	300	32.5	305	32.0	305	32.1	264	37.0	264	37.1	264	37.1
401.bzip2	489	19.8	486	19.9	489	19.7	493	19.6	494	19.6	493	19.6
403.gcc	291	27.7	290	27.8	290	27.7	282	28.6	288	28.0	283	28.4
429.mcf	181	50.5	176	51.9	175	52.2	180	50.7	176	51.7	177	51.6
445.gobmk	450	23.3	450	23.3	451	23.3	455	23.1	454	23.1	454	23.1
456.hammer	169	55.4	168	55.4	169	55.4	175	53.4	175	53.3	175	53.3
458.sjeng	433	27.9	433	27.9	433	27.9	432	28.0	432	28.0	432	28.0
462.libquantum	3.70	5600	3.67	5650	3.69	5610	3.70	5600	3.67	5650	3.69	5610
464.h264ref	568	39.0	566	39.1	568	38.9	568	39.0	566	39.1	568	38.9
471.omnetpp	212	29.5	197	31.7	199	31.5	151	41.3	152	41.1	153	40.9
473.astar	263	26.7	261	26.9	265	26.5	264	26.6	261	26.9	264	26.6
483.xalancbmk	131	52.5	132	52.3	132	52.4	133	52.1	132	52.3	132	52.1

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The config file option 'submit' was used.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

BIOS Configuraton:
Hyper-Threading Technology set to Disabled
CPU performance set to Enterprise
Power Technology set to Energy-Efficient
Energy Performance BIAS setting set to Balanced Performance
Memory RAS configuration set to Maximum Performance
LV DDR Mode set to Performance-mode
Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6914
\$Rev: 6914 \$ \$Date:: 2014-06-25 #\$ e3fbb8667b5a285932ceab81e28219e1
running on linux-616o Mon Aug 10 19:50:36 2015

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see: <http://www.spec.org/cpu2006/Docs/config.html#sysinfo>

```
From /proc/cpuinfo
model name : Intel(R) Xeon(R) CPU E5-4650 v3 @ 2.10GHz
4 "physical id"s (chips)
48 "processors"
```

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2015 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B420 M4 (Intel Xeon E5-4650 v3, 2.10 GHz)

SPECint2006 = 52.7

SPECint_base2006 = 51.1

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Aug-2015

Hardware Availability: Jun-2015

Software Availability: Nov-2014

Platform Notes (Continued)

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

```
cpu cores : 12
siblings  : 12
physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 13
physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 13
physical 2: cores 0 1 2 3 4 5 8 9 10 11 12 13
physical 3: cores 0 1 2 3 4 5 8 9 10 11 12 13
cache size : 30720 KB
```

From /proc/meminfo

```
MemTotal:      529334820 kB
HugePages_Total: 0
Hugepagesize:  2048 kB
```

From /etc/*release* /etc/*version*

SuSE-release:

SUSE Linux Enterprise Server 12 (x86_64)

VERSION = 12

PATCHLEVEL = 0

This file is deprecated and will be removed in a future service pack or release.

Please check /etc/os-release for details about this release.

os-release:

NAME="SLES"

VERSION="12"

VERSION_ID="12"

PRETTY_NAME="SUSE Linux Enterprise Server 12"

ID="sles"

ANSI_COLOR="0;32"

CPE_NAME="cpe:/o:suse:sles:12"

uname -a:

```
Linux linux-616o 3.12.28-4-default #1 SMP Thu Sep 25 17:02:34 UTC 2014
(9879bd4) x86_64 x86_64 x86_64 GNU/Linux
```

run-level 3 Aug 10 19:49

SPEC is set to: /opt/cpu2006-1.2

```
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sdc2        xfs   250G  11G  240G   5% /
```

Additional information from dmidecode:

Warning: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B420M4.2.2.5.0.043020152304 04/30/2015

Memory:

```
32x 0xCE00 M393A2G40DB0-CPB 16 GB 2 rank 2133 MHz
Continued on next page
```



SPEC CINT2006 Result

Copyright 2006-2015 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B420 M4 (Intel Xeon E5-4650 v3, 2.10 GHz)

SPECint2006 = 52.7

SPECint_base2006 = 51.1

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Aug-2015
Hardware Availability: Jun-2015
Software Availability: Nov-2014

Platform Notes (Continued)

16x NO DIMM NO DIMM

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:

KMP_AFFINITY = "granularity=fine,compact,1,0"

LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64:/opt/cpu2006-1.2/sh"

OMP_NUM_THREADS = "48"

Binaries compiled on a system with 1x Core i5-4670K CPU + 16GB memory using RedHat EL 7.0

Transparent Huge Pages enabled with:

echo always > /sys/kernel/mm/transparent_hugepage/enabled

Filesystem page cache cleared with:

echo 1> /proc/sys/vm/drop_caches

runspec command invoked through numactl i.e.:

numactl --interleave=all runspec <etc>

Base Compiler Invocation

C benchmarks:

icc -m64

C++ benchmarks:

icpc -m64

Base Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64

401.bzip2: -DSPEC_CPU_LP64

403.gcc: -DSPEC_CPU_LP64

429.mcf: -DSPEC_CPU_LP64

445.gobmk: -DSPEC_CPU_LP64

456.hmmer: -DSPEC_CPU_LP64

458.sjeng: -DSPEC_CPU_LP64

462.libquantum: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX

464.h264ref: -DSPEC_CPU_LP64

471.omnetpp: -DSPEC_CPU_LP64

473.astar: -DSPEC_CPU_LP64

483.xalanbmk: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX



SPEC CINT2006 Result

Copyright 2006-2015 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B420 M4 (Intel Xeon E5-4650 v3, 2.10 GHz)

SPECint2006 = 52.7

SPECint_base2006 = 51.1

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Aug-2015
Hardware Availability: Jun-2015
Software Availability: Nov-2014

Base Optimization Flags

C benchmarks:

`-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -opt-prefetch -auto-p32`

C++ benchmarks:

`-xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch -auto-p32
-Wl,-z,muldefs -L/sh -lsmartheap64`

Base Other Flags

C benchmarks:

`403.gcc: -Dalloca=_alloca`

Peak Compiler Invocation

C benchmarks (except as noted below):

`icc -m64`

`400.perlbench: icc -m32 -L/opt/intel/composer_xe_2015/lib/ia32`

`445.gobmk: icc -m32 -L/opt/intel/composer_xe_2015/lib/ia32`

C++ benchmarks (except as noted below):

`icpc -m32 -L/opt/intel/composer_xe_2015/lib/ia32`

`473.astar: icpc -m64`

Peak Portability Flags

`400.perlbench: -DSPEC_CPU_LINUX_IA32`

`401.bzip2: -DSPEC_CPU_LP64`

`403.gcc: -DSPEC_CPU_LP64`

`429.mcf: -DSPEC_CPU_LP64`

`456.hmmer: -DSPEC_CPU_LP64`

`458.sjeng: -DSPEC_CPU_LP64`

`462.libquantum: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX`

`464.h264ref: -DSPEC_CPU_LP64`

`473.astar: -DSPEC_CPU_LP64`

`483.xalancbmk: -DSPEC_CPU_LINUX`



SPEC CINT2006 Result

Copyright 2006-2015 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B420 M4 (Intel Xeon E5-4650 v3, 2.10 GHz)

SPECint2006 = 52.7

SPECint_base2006 = 51.1

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Aug-2015

Hardware Availability: Jun-2015

Software Availability: Nov-2014

Peak Optimization Flags

C benchmarks:

400.perlbench: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
 -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
 -opt-prefetch -ansi-alias

401.bzip2: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
 -O3(pass 2) -no-prec-div -prof-use(pass 2) -auto-ilp32
 -opt-prefetch -ansi-alias

403.gcc: -xCORE-AVX2 -ipo -O3 -no-prec-div -inline-calloc
 -opt-malloc-options=3 -auto-ilp32

429.mcf: -xCORE-AVX2 -ipo -O3 -no-prec-div -parallel
 -opt-prefetch -auto-p32

445.gobmk: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -prof-use(pass 2)
 -ansi-alias

456.hmmer: -xCORE-AVX2 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32
 -ansi-alias

458.sjeng: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
 -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
 -unroll4

462.libquantum: basepeak = yes

464.h264ref: basepeak = yes

C++ benchmarks:

471.omnetpp: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
 -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
 -opt-ra-region-strategy=block -ansi-alias
 -Wl,-z,muldefs -L/sh -lsmarheap

473.astar: -xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch
 -auto-p32 -Wl,-z,muldefs -L/sh -lsmarheap64

483.xalancbmk: -xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch
 -ansi-alias -Wl,-z,muldefs -L/sh -lsmarheap

Peak Other Flags

C benchmarks:

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2015 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B420 M4 (Intel Xeon E5-4650 v3, 2.10 GHz)

SPECint2006 = 52.7

SPECint_base2006 = 51.1

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Aug-2015

Hardware Availability: Jun-2015

Software Availability: Nov-2014

Peak Other Flags (Continued)

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2006/flags/Intel-ic15.0-official-linux64.html>

<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revC.20150812.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2006/flags/Intel-ic15.0-official-linux64.xml>

<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revC.20150812.xml>

SPEC and SPECint are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.
Report generated on Tue Aug 25 17:54:01 2015 by SPEC CPU2006 PS/PDF formatter v6932.
Originally published on 25 August 2015.