SPEC® CINT2006 Result
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Cisco Systems

Cisco UCS C420 M3 (Intel Xeon E5-4620, 2.20 GHz)

SPECint®_rate2006 = 1010
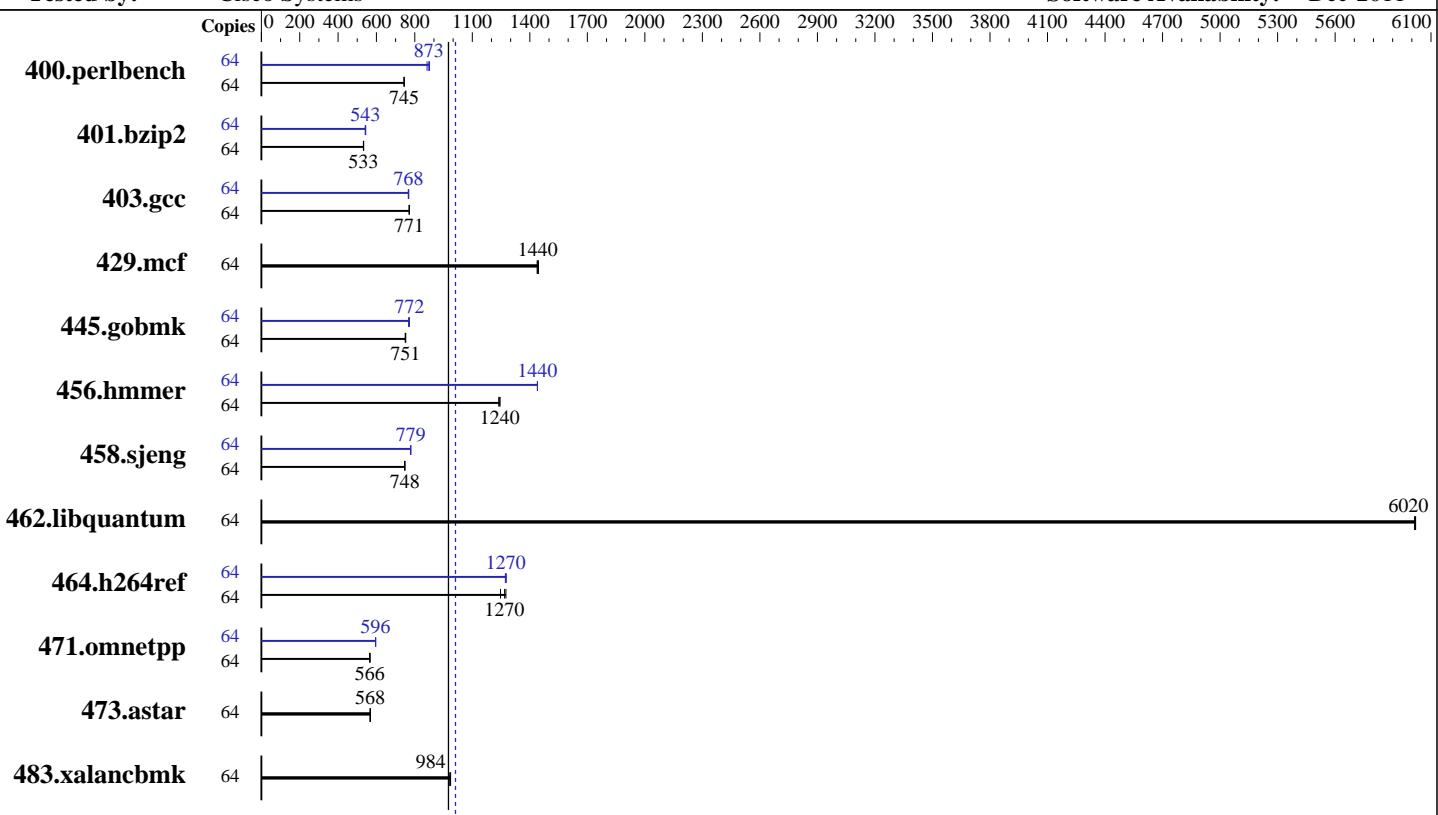
SPECint_rate_base2006 = 976

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: May-2013
Hardware Availability: Nov-2012
Software Availability: Dec-2011

Copies 0 200 400 600 800 1100 1400 1700 2000 2300 2600 2900 3200 3500 3800 4100 4400 4700 5000 5300 5600 6100

```
400.perlbench    64    873
                 64    745
401.bzip2        64    543
                 64    533
403.gcc          64    768
                 64    771
429.mcf          64    1440
445.gobmk        64    772
                 64    751
456.hmmer        64    1440
                 64    1240
458.sjeng        64    779
                 64    748
462.libquantum   64    6020
464.h264ref      64    1270
                 64    1270
471.omnetpp      64    596
                 64    566
473.astar        64    568
483.xalancbmk    64    984
```

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Hardware

CPU Name:	Intel Xeon E5-4620
CPU Characteristics:	Intel Turbo Boost Technology up to 2.60 GHz
CPU MHz:	2200
FPU:	Integrated
CPU(s) enabled:	32 cores, 4 chips, 8 cores/chip, 2 threads/core
CPU(s) orderable:	1,2,3,4 chips
Primary Cache:	32 KB I + 32 KB D on chip per core
Secondary Cache:	256 KB I+D on chip per core
L3 Cache:	16 MB I+D on chip per chip
Other Cache:	None
Memory:	256 GB (32 x 8 GB 2Rx4 PC3-12800R-11, ECC)
Disk Subsystem:	1 X 600GB SAS, 10K RPM
Other Hardware:	None

Software

Operating System:	Red Hat Enterprise Linux Server release 6.2 (Santiago) 2.6.32-220.el6.x86_64
Compiler:	C/C++: Version 12.1.3.293 of Intel C++ Studio XE for Linux
Auto Parallel:	No
File System:	ext4
System State:	Run level 3 (multi-user)
Base Pointers:	32-bit
Peak Pointers:	32/64-bit
Other Software:	Microquill SmartHeap V9.01

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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	64	839	745	**839**	**745**	841	744	64	713	877	**716**	**873**	724	864
401.bzip2	64	1161	532	**1159**	**533**	1158	533	64	1135	544	**1138**	**543**	1140	542
403.gcc	64	**668**	**771**	667	772	669	771	64	673	766	**671**	**768**	670	768
429.mcf	64	**405**	**1440**	406	1440	404	1450	64	**405**	**1440**	406	1440	404	1450
445.gobmk	64	895	750	**893**	**751**	892	753	64	875	768	**870**	**772**	870	772
456.hmmer	64	482	1240	480	1240	**480**	**1240**	64	415	1440	**415**	**1440**	415	1440
458.sjeng	64	**1035**	**748**	1036	748	1035	748	64	995	779	**994**	**779**	994	779
462.libquantum	64	221	6010	220	6020	**220**	**6020**	64	221	6010	220	6020	**220**	**6020**
464.h264ref	64	1110	1280	1136	1250	**1117**	**1270**	64	**1111**	**1270**	1109	1280	1113	1270
471.omnetpp	64	708	565	**707**	**566**	706	567	64	672	595	**672**	**596**	671	596
473.astar	64	**791**	**568**	793	567	791	568	64	**791**	**568**	793	567	791	568
483.xalancbmk	64	447	987	449	983	**449**	**984**	64	447	987	449	983	**449**	**984**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

    The numactl mechanism was used to bind copies to processors. The config file option 'submit'
    was used to generate numactl commands to bind each copy to a specific processor.
    For details, please see the config file.

Operating System Notes

    Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

    BIOS Settings:
    Power Technology set to Custom
    Processor Power State C6 set to Disabled
    Processor Power State C1 Enhanced set to Disabled
    Energy Performance Set to Performance
    DRAM Clock Throttling Set to Performance

     Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6800
     $Rev: 6800 $ $Date:: 2011-10-11 #$ 6f2ebdff5032aaa42e583f96b07f99d3
     running on localhost.localdomain Fri May 31 14:55:47 2013

     This section contains SUT (System Under Test) info as seen by
     some common utilities. To remove or add to this section, see:
       http://www.spec.org/cpu2006/Docs/config.html#sysinfo

     From /proc/cpuinfo
        model name : Intel(R) Xeon(R) CPU E5-4620 0 @ 2.20GHz

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Platform Notes (Continued)

```
     4 "physical id"s (chips)
     64 "processors"
  cores, siblings (Caution: counting these is hw and system dependent.  The
  following excerpts from /proc/cpuinfo might not be reliable.  Use with
  caution.)
     cpu cores : 8
     siblings  : 16
     physical 0: cores 0 1 2 3 4 5 6 7
     physical 1: cores 0 1 2 3 4 5 6 7
     physical 2: cores 0 1 2 3 4 5 6 7
     physical 3: cores 0 1 2 3 4 5 6 7
  cache size : 16384 KB

From /proc/meminfo
   MemTotal:        264502996 kB
   HugePages_Total:        0
   Hugepagesize:        2048 kB

/usr/bin/lsb_release -d
   Red Hat Enterprise Linux Server release 6.2 (Santiago)

From /etc/*release* /etc/*version*
   redhat-release: Red Hat Enterprise Linux Server release 6.2 (Santiago)
   system-release: Red Hat Enterprise Linux Server release 6.2 (Santiago)
   system-release-cpe: cpe:/o:redhat:enterprise_linux:6server:ga:server

uname -a:
   Linux localhost.localdomain 2.6.32-220.el6.x86_64 #1 SMP Wed Nov 9 08:03:13
   EST 2011 x86_64 x86_64 x86_64 GNU/Linux

run-level 3 May 31 14:52

SPEC is set to: /opt/cpu2006-1.2
   Filesystem     Type     Size  Used Avail Use% Mounted on
   /dev/sda1      ext4     134G   27G  101G  22% /

Additional information from dmidecode:
  Memory:
   32x 0xCE00 M393B1K70DH0-YK0 8 GB 1600 MHz 2 rank

(End of data from sysinfo program)
```

General Notes

```
Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64"

 Binaries compiled on a system with 2 X Intel Xeon E5-2690 CPU + 128 GB memory
 using RHEL 6.2
 Transparent Huge Pages enabled with:
 echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled
```

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General Notes (Continued)

```
 Filesystem page cache cleared with:
 echo 1>        /proc/sys/vm/drop_caches
```

Base Compiler Invocation

C benchmarks:
```
    icc  -m32
```

C++ benchmarks:
```
    icpc -m32
```

Base Portability Flags

```
    400.perlbench: -DSPEC_CPU_LINUX_IA32
    462.libquantum: -DSPEC_CPU_LINUX
    483.xalancbmk: -DSPEC_CPU_LINUX
```

Base Optimization Flags

C benchmarks:
```
    -xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3
```

C++ benchmarks:
```
    -xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3
    -Wl,-z,muldefs -L/smartheap -lsmartheap
```

Base Other Flags

C benchmarks:

```
        403.gcc: -Dalloca=_alloca
```

Peak Compiler Invocation

C benchmarks (except as noted below):
```
    icc  -m32
```

```
    400.perlbench: icc -m64
```

```
      401.bzip2: icc -m64
```

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Peak Compiler Invocation (Continued)

456.hmmer: `icc -m64`

458.sjeng: `icc -m64`

C++ benchmarks:
`icpc -m32`

Peak Portability Flags

400.perlbench: `-DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64`
401.bzip2: `-DSPEC_CPU_LP64`
456.hmmer: `-DSPEC_CPU_LP64`
458.sjeng: `-DSPEC_CPU_LP64`
462.libquantum: `-DSPEC_CPU_LINUX`
483.xalancbmk: `-DSPEC_CPU_LINUX`

Peak Optimization Flags

C benchmarks:

400.perlbench: `-xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)`
`-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)`
`-auto-ilp32`

401.bzip2: `-xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)`
`-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)`
`-opt-prefetch -auto-ilp32 -ansi-alias`

403.gcc: `-xSSE4.2 -ipo -O3 -no-prec-div`

429.mcf: `basepeak = yes`

445.gobmk: `-xSSE4.2(pass 2) -prof-gen(pass 1) -prof-use(pass 2)`
`-ansi-alias -opt-mem-layout-trans=3`

456.hmmer: `-xSSE4.2 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32`

458.sjeng: `-xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)`
`-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)`
`-unroll4 -auto-ilp32`

462.libquantum: `basepeak = yes`

464.h264ref: `-xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)`
`-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)`
`-unroll2 -ansi-alias`

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Peak Optimization Flags (Continued)

C++ benchmarks:

471.omnetpp: `-xSSE4.2(pass 2)` `-prof-gen(pass 1)` `-ipo(pass 2)`
`-O3(pass 2)` `-no-prec-div(pass 2)` `-prof-use(pass 2)`
`-ansi-alias` `-opt-ra-region-strategy=block` `-Wl,-z,muldefs`
`-L/smartheap` `-lsmartheap`

473.astar: `basepeak = yes`

483.xalancbmk: `basepeak = yes`

Peak Other Flags

C benchmarks:

403.gcc: `-Dalloca=_alloca`

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic12.1-official-linux64.20120425.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130717.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic12.1-official-linux64.20120425.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130717.xml

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.
Report generated on Thu Jul 24 16:30:56 2014 by SPEC CPU2006 PS/PDF formatter v6932.
Originally published on 17 July 2013.