



SPEC® CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C420 M3 (Intel Xeon E5-4640, 2.40 GHz)

SPECint_rate2006 = 1090

SPECint_rate_base2006 = 1050

CPU2006 license: 9019

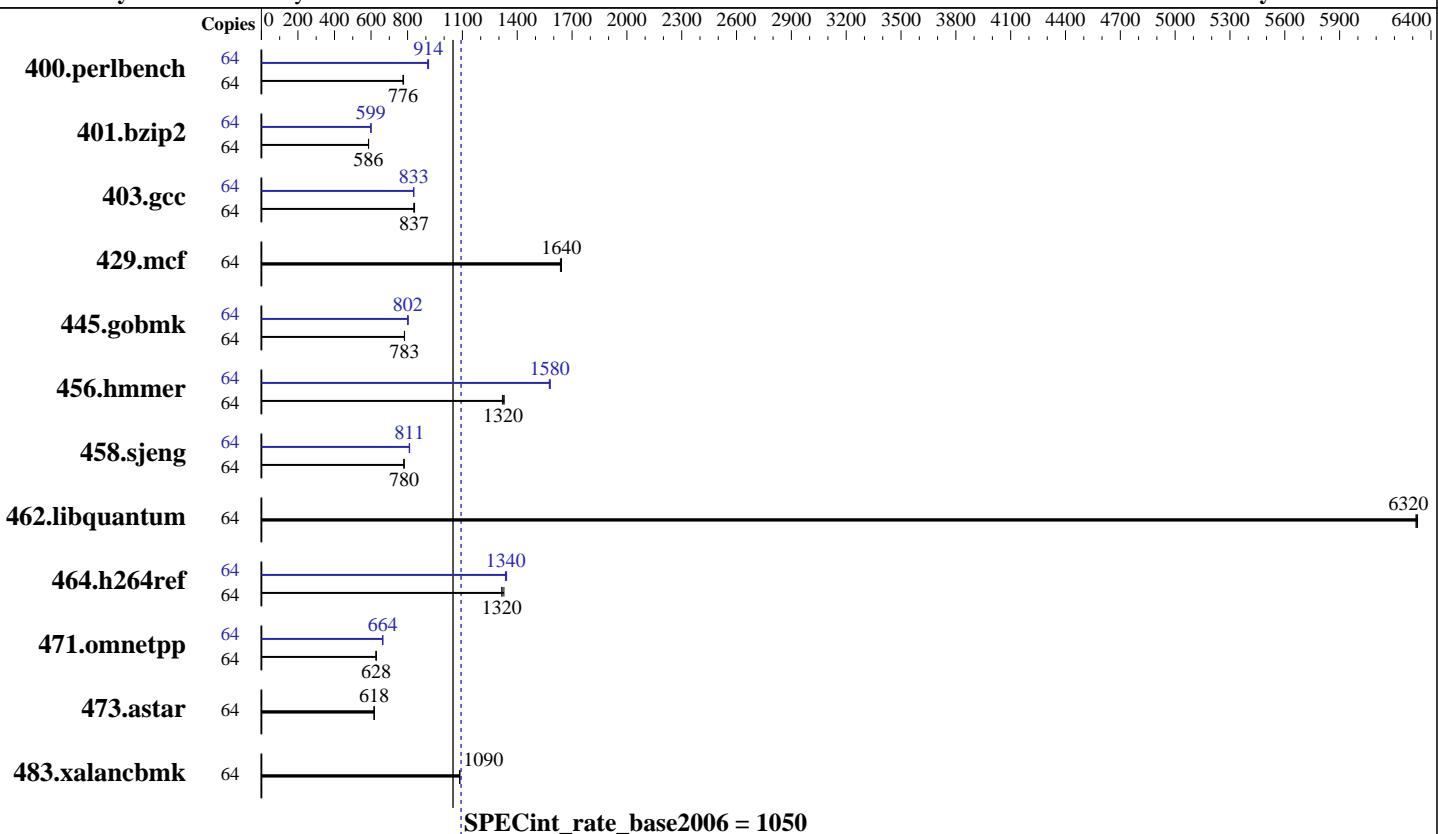
Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: May-2013

Hardware Availability: Nov-2012

Software Availability: Dec-2011



Hardware

CPU Name:	Intel Xeon E5-4640
CPU Characteristics:	Intel Turbo Boost Technology up to 2.80 GHz
CPU MHz:	2400
FPU:	Integrated
CPU(s) enabled:	32 cores, 4 chips, 8 cores/chip, 2 threads/core
CPU(s) orderable:	1,2,3,4 chip
Primary Cache:	32 KB I + 32 KB D on chip per core
Secondary Cache:	256 KB I+D on chip per core
L3 Cache:	20 MB I+D on chip per chip
Other Cache:	None
Memory:	256 GB (32 x 8 GB 2Rx4 PC3-12800R-11, ECC)
Disk Subsystem:	1 X 600GB SAS, 10K RPM
Other Hardware:	None

Software

Operating System:	Red Hat Enterprise Linux Server release 6.3 (Santiago) 2.6.32-279.el6.x86_64
Compiler:	C/C++: Version 12.1.3.293 of Intel C++ Studio XE for Linux
Auto Parallel:	No
File System:	ext4
System State:	Run level 3 (multi-user)
Base Pointers:	32-bit
Peak Pointers:	32/64-bit
Other Software:	Microquill SmartHeap V9.01



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C420 M3 (Intel Xeon E5-4640, 2.40 GHz)

SPECint_rate2006 = 1090

SPECint_rate_base2006 = 1050

CPU2006 license: 9019

Test date: May-2013

Test sponsor: Cisco Systems

Hardware Availability: Nov-2012

Tested by: Cisco Systems

Software Availability: Dec-2011

Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	64	806	776	804	778	806	775	64	684	914	687	910	683	915
401.bzip2	64	1053	586	1053	587	1054	586	64	1030	599	1030	599	1030	600
403.gcc	64	616	837	618	834	615	838	64	618	834	618	833	618	833
429.mcf	64	357	1640	356	1640	355	1640	64	357	1640	356	1640	355	1640
445.gobmk	64	858	783	857	783	858	783	64	836	803	837	802	838	801
456.hmmer	64	453	1320	451	1320	449	1330	64	378	1580	378	1580	379	1580
458.sjeng	64	992	780	992	781	992	780	64	957	809	955	811	955	811
462.libquantum	64	210	6330	210	6320	210	6320	64	210	6330	210	6320	210	6320
464.h264ref	64	1076	1320	1067	1330	1076	1320	64	1058	1340	1061	1340	1056	1340
471.omnetpp	64	637	628	637	628	637	628	64	603	664	602	665	603	663
473.astar	64	729	616	727	618	727	618	64	729	616	727	618	727	618
483.xalancbmk	64	407	1080	407	1090	407	1090	64	407	1080	407	1090	407	1090

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

BIOS Settings:

Power Technology set to Custom

Processor Power State C6 set to Disabled

Processor Power State C1 Enhanced set to Disabled

Energy Performance Set to Performance

DRAM Clock Throttling Set to Performance

```
Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6800
$Rev: 6800 $ $Date:: 2011-10-11 #$
running on SPECCPU-RHEL6.3 Thu May 16 23:32:39 2013
```

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
<http://www.spec.org/cpu2006/Docs/config.html#sysinfo>

```
From /proc/cpuinfo
model name : Intel(R) Xeon(R) CPU E5-4640 0 @ 2.40GHz
Continued on next page
```



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C420 M3 (Intel Xeon E5-4640, 2.40 GHz)

SPECint_rate2006 = 1090

SPECint_rate_base2006 = 1050

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: May-2013

Hardware Availability: Nov-2012

Software Availability: Dec-2011

Platform Notes (Continued)

```
4 "physical id"s (chips)
 64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The
following excerpts from /proc/cpuinfo might not be reliable. Use with
caution.)
  cpu cores : 8
  siblings   : 16
  physical 0: cores 0 1 2 3 4 5 6 7
  physical 1: cores 0 1 2 3 4 5 6 7
  physical 2: cores 0 1 2 3 4 5 6 7
  physical 3: cores 0 1 2 3 4 5 6 7
cache size : 20480 KB

From /proc/meminfo
MemTotal:      264502612 kB
HugePages_Total:       0
Hugepagesize:     2048 kB

/usr/bin/lsb_release -d
Red Hat Enterprise Linux Server release 6.3 (Santiago)

From /etc/*release* /etc/*version*
redhat-release: Red Hat Enterprise Linux Server release 6.3 (Santiago)
system-release: Red Hat Enterprise Linux Server release 6.3 (Santiago)
system-release-cpe: cpe:/o:redhat:enterprise_linux:6server:ga:server

uname -a:
Linux SPECCPU-RHEL6.3 2.6.32-279.el6.x86_64 #1 SMP Wed Jun 13 18:24:36 EDT
2012 x86_64 x86_64 x86_64 GNU/Linux

run-level 3 May 16 16:21

SPEC is set to: /opt/cpu2006-1.2
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sda2        ext4  274G  9.4G  251G  4%  /

Additional information from dmidecode:
Memory:
 32x 0xCE00 M393B1K70DH0-YK0 8 GB 1600 MHz 2 rank

(End of data from sysinfo program)
```

General Notes

Environment variables set by runspec before the start of the run:

LD_LIBRARY_PATH = "/opt/cpu2006-1.2/lib32:/opt/cpu2006-1.2/lib64"

Binaries compiled on a system with 2 X Intel Xeon E5-2690 CPU + 128 GB memory
using RHEL 6.2

Transparent Huge Pages enabled with:

echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C420 M3 (Intel Xeon E5-4640, 2.40 GHz)

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

SPECint_rate2006 = 1090

SPECint_rate_base2006 = 1050

Test date: May-2013

Hardware Availability: Nov-2012

Software Availability: Dec-2011

General Notes (Continued)

Filesystem page cache cleared with:
echo 1> /proc/sys/vm/drop_caches

Base Compiler Invocation

C benchmarks:

icc -m32

C++ benchmarks:

icpc -m32

Base Portability Flags

400.perlbench: -DSPEC_CPU_LINUX_IA32

462.libquantum: -DSPEC_CPU_LINUX

483.xalancbmk: -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:

-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3

C++ benchmarks:

-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3
-Wl,-z,muldefs -L/smartheap -lsmartheap

Base Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):

icc -m32

400.perlbench: icc -m64

401.bzip2: icc -m64

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C420 M3 (Intel Xeon E5-4640, 2.40 GHz)

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

SPECint_rate2006 = 1090

SPECint_rate_base2006 = 1050

Test date: May-2013

Hardware Availability: Nov-2012

Software Availability: Dec-2011

Peak Compiler Invocation (Continued)

456.hmmer: icc -m64

458.sjeng: icc -m64

C++ benchmarks:

icpc -m32

Peak Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64

401.bzip2: -DSPEC_CPU_LP64

456.hmmer: -DSPEC_CPU_LP64

458.sjeng: -DSPEC_CPU_LP64

462.libquantum: -DSPEC_CPU_LINUX

483.xalancbmk: -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:

400.perlbench: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-auto-ilp32

401.bzip2: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-opt-prefetch -auto-ilp32 -ansi-alias

403.gcc: -xSSE4.2 -ipo -O3 -no-prec-div

429.mcf: basepeak = yes

445.gobmk: -xSSE4.2(pass 2) -prof-gen(pass 1) -prof-use(pass 2)
-ansi-alias -opt-mem-layout-trans=3

456.hmmer: -xSSE4.2 -ipo -O3 -no-prec-div -unroll12 -auto-ilp32

458.sjeng: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-unroll14 -auto-ilp32

462.libquantum: basepeak = yes

464.h264ref: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-unroll12 -ansi-alias

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C420 M3 (Intel Xeon E5-4640, 2.40 GHz)

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

SPECint_rate2006 = 1090

SPECint_rate_base2006 = 1050

Test date: May-2013

Hardware Availability: Nov-2012

Software Availability: Dec-2011

Peak Optimization Flags (Continued)

C++ benchmarks:

```
471.omnetpp: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
             -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
             -ansi-alias -opt-ra-region-strategy=block -Wl,-z,muldefs
             -L/smarterheap -lsmarterheap
```

```
473.astar: basepeak = yes
```

```
483.xalancbmk: basepeak = yes
```

Peak Other Flags

C benchmarks:

```
403.gcc: -Dalloca=_alloca
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2006/flags/Intel-ic12.1-official-linux64.20120425.html>
<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130607.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2006/flags/Intel-ic12.1-official-linux64.20120425.xml>
<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130607.xml>

SPEC and SPECint are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.

Report generated on Thu Jul 24 15:31:54 2014 by SPEC CPU2006 PS/PDF formatter v6932.

Originally published on 7 June 2013.