



Standard Performance Evaluation Corporation (SPEC)

# Server Efficiency Rating Tool (SERT®) Platform Enablement and Acceptance Process

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Latest SERT 2.x.x version: [https://www.spec.org/sert2/SERT-platform\\_acceptance\\_process.pdf](https://www.spec.org/sert2/SERT-platform_acceptance_process.pdf)

## 1. Overview

The Server Efficiency Rating Tool (SERT) suite was created by the Standard Performance Evaluation Corporation (SPEC), the world's leading organization for benchmarking expertise. The SPECpower Committee designed, implemented, and delivered the SERT suite, a next-generation tool set for measuring and evaluating the energy efficiency of servers. The SERT suite was created with input from leaders of various global energy-efficiency programs and their stakeholders in order to accommodate their regional program requirements.

### 1.1. Introduction

This document describes the platform enablement and acceptance process for the SERT suite. It specifically describes the steps needed to add support to the SERT suite for all types of new platforms.

The enablement and acceptance process is reasonably straightforward, and can be initiated by the processor vendor, or an authorized OEM/ODM that ships platforms based on the processor for which acceptance is needed. Virtually any platform/architecture combination can acquire SERT support.

Platform acceptance for x86, ARM, Itanium, SPARC or POWER architectures running Windows or Linux is usually light weight. All that is needed is completion of the tests described in ISO/IEC 21836:2020 9.3 (<https://www.iso.org/standard/71926.html>), using the, simple to follow, questionnaire-based spreadsheet provided by SPEC.

For platforms not using CPUs of the above-mentioned architectures, the SERT enablement requires updates to the Discovery Scripts and porting of the Storage Subsystem native code.

The SERT suite is designed to work on virtually all servers and requires the use of a Java Virtual machine (JVM).

Obtaining the SERT support is a twostep process, Enablement and Acceptance. To request platform acceptance from SPEC, the SERT suite must be enabled on the platform first. The remainder of this document describes both the Enablement and Acceptance processes.

### 1.2. Trademark and Copyright Notice

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## 2. Platform Enablement

This section describes the process of Enabling SERT support for a platform. This enablement step is needed only for platforms that are not derived from an accepted CPU architecture and operating system (OS), with a configuration in SPEC's "Client Configurations" file (see: <https://www.spec.org/sert2/client-configurations-2.0.xml>). For all other platforms, please proceed directly to the *Platform Acceptance* section.

### 2.1. What is Enablement?

Even though nearly all the tests run by the SERT suite are Java based and only require an installed Java Virtual Machine, the SERT Storage Workload is written using native code and requires porting. Also, updates to the SERT Discovery scripts, which provide system configuration information, are typically required.

A vendor or authorized OEM/ODM can initiate platform enablement by sending a request via (<https://www.spec.org/sert/feedback/issuereport.html>).

#### 2.1.1. Native Code

The SERT Storage Workload is written using native code which must be compiled for the new platform. This binary is invoked by the SERT suite to run the SERT Storage Workload. The SPECpower committee can provide guidance on porting and compiling this code.

#### 2.1.2. Discovery Scripts

When the SERT suite is run on a system, it initiates a "discovery" process. This process programmatically examines the system configuration to determine system details the SERT suite uses to configure the run. Some configuration details are also used for automatic configuration documentation.

## 3. Platform Acceptance

Platform acceptance is the process by which a platform vendor or authorized OEM/ODM can request a given platform to be accepted by SPEC and it's definition be published via the list of accepted platforms (<https://www.spec.org/sert2/client-configurations-2.0.xml>).

### 3.1. What is Acceptance?

Acceptance is the process by which a platform vendor or authorized OEM/ODM demonstrates compliance with the requirements of ISO/IEC 21836:2020 by showing the SPECpower committee the expected scaling and functionality on their platform.

The acceptance process does not require any absolute platform performance or power data to be shared with SPEC. Only relative deviation and scaling between successive runs of the SERT suite is shared with SPEC. The processor model number, the OS name and version, and the JVM vendor and version number, are shared with SPEC as the basis for the platform to be added to the accepted platforms list (<https://www.spec.org/sert2/client-configurations-2.0.xml>).

### 3.2. Acceptance Process

The acceptance process is defined in the ISO/IEC 21836:2020 standard and describes the different test cases that need to be run with the SERT suite. This document does not repeat the details, but rather provides a high-level overview of what to expect.

In general, the Platform Acceptance seeker needs to run a set of tests to demonstrate that their platform and OS and JVM options result in consistent SERT runs with minimal deviation in performance between successive runs, and the relative performance scales as expected with varying system hardware resources. There are four main acceptance categories as described below.

### 3.3. Seeking Acceptance for a new platform

The following are the set of ISO/IEC 21836:2020 test plans used for platform acceptance. For definitions of terms and full details on the tests, please see ISO/IEC 21836:2020.

#### 3.3.1. New CPU Architecture Classes

This test plan includes the most tests because it is intended for completely new CPU architecture classes.

1. CPU Sockets: if more than one socket is supported by the platform, tests need to be run with different number of CPU sockets populated.
2. CPU Frequency: if processor SKUs are sold with different operating frequencies, tests need to be run with SKUs of varying frequency.
3. CPU Core Count: if processor SKUs are sold with different number of cores, tests need to be run with SKUs with varying number of cores.
4. Memory Size Test: if the platform supports different total memory population, tests need to be run with varying amount of memory installed.
5. Memory Frequency Test: if the platform supports different memory operating frequencies (speed), then tests need to be run with varying memory frequency.
6. Storage Quantity Test: if the platform supports more than one storage device, then tests need to be run with varying number of storage devices.
7. Storage Technology: if the platform supports more than one type of storage technology, then tests need to be run with different types of storage devices installed.
8. Validity and Variance: set of 5 consecutive runs of the SERT suite need to be run, and those tests cannot show more than 10% variation in performance among them.

#### 3.3.2. New Software acceptance for accepted CPU Architectures

This test plan is used to gain acceptance of new software on platforms with an already accepted CPU architecture.

1. CPU Sockets - if more than one socket is supported by the platform, tests need to be run with different number of CPU sockets populated.
2. Memory Size Test: if the platform supports different total memory population, tests need to be run with varying amount of memory installed.
3. Storage Quantity Test: if the platform supports more than one storage device, then tests need to be run with varying number of storage devices.
4. Storage Technology: if the platform supports more than one type of storage technology, then tests need to be run with different types of storage devices installed.
5. Validity and Variance: set of 5 consecutive runs of the SERT suite need to be run, and those tests cannot show more than 10% variation in performance among them.

#### 3.3.3. If the Software in 3.3.2 is a minor change

This test plan is used for minor updates to accepted CPU architectures, OSES, and JVM.

1. Validity and Variance: set of 5 consecutive runs of the SERT suite need to be run, and those tests cannot show more than 10% variation in performance among them.

### **3.3.4. New CPU Architecture from an already accepted CPU Architecture Class**

This test plan is used to gain acceptance for a new CPU architecture in an accepted CPU architecture family.

1. CPU Sockets: if more than one socket is supported by the platform, tests need to be run with different number of CPU sockets populated.
2. CPU Core Count: if processor SKUs are sold with different number of cores, tests need to be run with SKUs with varying number of cores.
3. Memory Size Test: if the platform supports different total memory population, tests need to be run with varying amount of memory installed.
4. Validity and Variance: set of 5 consecutive runs of the SERT suite need to be run, and those tests cannot show more than 10% variation in performance among them.

### **3.3.5. New CPU Model from an already accepted CPU Architecture**

This test plan is used to gain acceptance for new CPU models in an accepted CPU architecture.

1. Validity and Variance: set of 5 consecutive runs of the SERT suite need to be run, and those tests cannot show more than 10% variation in performance among them.

### **3.3.6. Submitting Data to SPEC for acceptance**

Once the tests are complete for the above scenarios, the vendor or authorized representative can populate the platform acceptance spreadsheet provided by SPEC. The use of absolute benchmark scores is not required, and relative data between tests can be used.

The Spreadsheet includes fields which need to be filled out that identify the processor, OS and JVM used for the tests.

Once a platform is accepted by SPEC, the client configuration file (<https://www.spec.org/sert2/client-configurations-2.0.xml>) is updated with the new platform information, and published on SPEC's website.

## **4. Conclusion**

This document lays out a high-level view of the SERT Enablement and Acceptance process. Key items documented in this document include:

1. SPEC SERT suite is designed to work on a wide variety of platforms.
2. For platforms with CPUs in the accepted CPU Architecture Classes, enabling a new platform to run the SERT suite requires minimal effort
3. For platforms that use CPU with a new CPU Architecture Class, two SERT components need to be updated, and SPEC can provide update support.
4. Virtually any server can be enabled and accepted.
5. Any platform vendor, or their authorized OEM/ODM/Resellers, can request platform enablement and acceptance.
6. No absolute performance data or confidential information is shared with SPEC during this process.
7. SPEC offers special assistance to any company seeking to obtain SERT platform support, according to ISO/IEC 21836:2020 9.3.