



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2022 Standard Performance Evaluation Corporation

Hewlett Packard Enterprise

(Test Sponsor: HPE)

ProLiant DL20 Gen10 Plus

(3.20 GHz, Intel Xeon E-2356G)

SPECrate®2017_int_base = 59.0

SPECrate®2017_int_peak = 61.6

CPU2017 License: 3

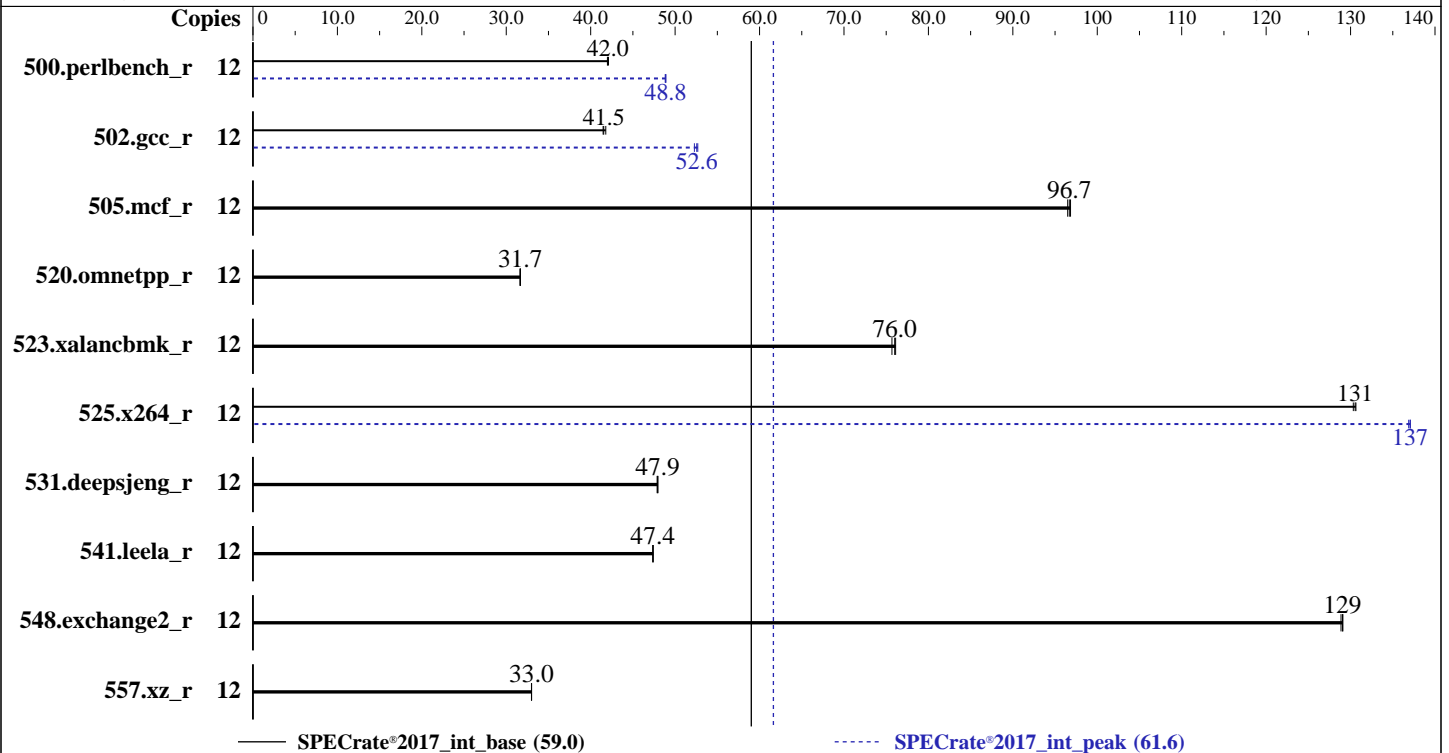
Test Sponsor: HPE

Tested by: HPE

Test Date: Mar-2022

Hardware Availability: Jan-2022

Software Availability: Jun-2021



Hardware

CPU Name: Intel Xeon E-2356G
 Max MHz: 5000
 Nominal: 3200
 Enabled: 6 cores, 1 chip, 2 threads/core
 Orderable: 1 chip
 Cache L1: 32 KB I + 48 KB D on chip per core
 L2: 512 KB I+D on chip per core
 L3: 12 MB I+D on chip per chip
 Other: None
 Memory: 128 GB (4 x 32 GB 2Rx8 PC4-3200AA-E, running at 2933)
 Storage: 1 x 480 GB SATA SSD, RAID 0
 Other: None

Software

OS: SUSE Linux Enterprise Server 15 SP3
 Kernel 5.3.18-57-default
 Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux;
 Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;
 C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux
 Parallel: No
 Firmware: HPE BIOS Version U60 v1.54 01/13/2022 released Jan-2022
 File System: xfs
 System State: Run level 3 (multi-user)
 Base Pointers: 64-bit
 Peak Pointers: 32/64-bit
 Other: jemalloc memory allocator V5.0.1
 Power Management: BIOS set to prefer performance at the cost of additional power usage



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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
500.perlbench_r	12	454	42.1	455	42.0	455	42.0	12	391	48.8	391	48.8	391	48.9
502.gcc_r	12	409	41.5	407	41.8	410	41.5	12	323	52.7	323	52.6	325	52.3
505.mcf_r	12	201	96.5	200	96.8	201	96.7	12	201	96.5	200	96.8	201	96.7
520.omnetpp_r	12	497	31.7	498	31.6	497	31.7	12	497	31.7	498	31.6	497	31.7
523.xalancbmk_r	12	167	76.0	167	75.7	166	76.1	12	167	76.0	167	75.7	166	76.1
525.x264_r	12	161	130	161	131	161	131	12	154	137	153	137	153	137
531.deepsjeng_r	12	287	48.0	287	47.9	287	47.9	12	287	48.0	287	47.9	287	47.9
541.leela_r	12	419	47.4	420	47.4	419	47.4	12	419	47.4	420	47.4	419	47.4
548.exchange2_r	12	244	129	244	129	244	129	12	244	129	244	129	244	129
557.xz_r	12	393	33.0	393	33.0	393	33.0	12	393	33.0	393	33.0	393	33.0

SPECrate®2017_int_base = **59.0**

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

```
Stack size set to unlimited using "ulimit -s unlimited"
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches
```

Environment Variables Notes

```
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH =
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"
MALLOC_CONF = "retain:true"
```

General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Red Hat Enterprise Linux 8.1
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)

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General Notes (Continued)

is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation

built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

Platform Notes

BIOS Configuration:

Workload Profile set to General Throughput Compute

Thermal Configuration set to Maximum Cooling

Enhanced Processor Performance set to Enabled

Last Level Cache (LLC) prefetch set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo

Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d

running on localhost Tue Mar 8 13:53:30 2022

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

model name : Intel(R) Xeon(R) E-2356G CPU @ 3.20GHz

1 "physical id"s (chips)

12 "processors"

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

cpu cores : 6

siblings : 12

physical 0: cores 0 1 2 3 4 5

From lscpu from util-linux 2.36.2:

Architecture: x86_64

CPU op-mode(s): 32-bit, 64-bit

Byte Order: Little Endian

Address sizes: 39 bits physical, 48 bits virtual

CPU(s): 12

On-line CPU(s) list: 0-11

Thread(s) per core: 2

Core(s) per socket: 6

Socket(s): 1

NUMA node(s): 1

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Platform Notes (Continued)

```

Vendor ID: GenuineIntel
CPU family: 6
Model: 167
Model name: Intel(R) Xeon(R) E-2356G CPU @ 3.20GHz
Stepping: 1
CPU MHz: 4805.132
BogoMIPS: 6384.00
Virtualization: VT-x
L1d cache: 288 KiB
L1i cache: 192 KiB
L2 cache: 3 MiB
L3 cache: 12 MiB
NUMA node0 CPU(s): 0-11
Vulnerability Itlb multihit: Not affected
Vulnerability L1tf: Not affected
Vulnerability Mds: Not affected
Vulnerability Meltdown: Not affected
Vulnerability Spec store bypass: Mitigation; Speculative Store Bypass disabled via prctl and seccomp
Vulnerability Spectre v1: Mitigation; usercopy/swapgs barriers and __user pointer sanitization
Vulnerability Spectre v2: Mitigation; Enhanced IBRS, IBPB conditional, RSB filling
Vulnerability Srbds: Not affected
Vulnerability Tsx async abort: Not affected
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr
pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx
pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology
nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx
smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb invpcid_single ssbd ibrs_ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority
ept vpid ept_ad fsgsbase tsc_adjust bmi1 avx2 smep bmi2 erms invpcid mpx avx512f
avx512dq rdseed adx smap avx512ifma clflushopt intel_pt avx512cd sha_ni avx512bw
avx512vl xsaveopt xsavec xgetbv1 xsaves dtherm ida arat pln pts avx512vbmi umip pku
ospke avx512_vbmi2 gfni vaes vpclmulqdq avx512_vnni avx512_bitalg avx512_vpopcntdq
rdpid fsrm md_clear flush_lld arch_capabilities

```

From lscpu --cache:

NAME	ONE-SIZE	ALL-SIZE	WAYS	TYPE	LEVEL	SETS	PHY-LINE	COHERENCY-SIZE
L1d	48K	288K	12	Data	1	64	1	64
L1i	32K	192K	8	Instruction	1	64	1	64
L2	512K	3M	8	Unified	2	1024	1	64
L3	12M	12M	16	Unified	3	12288	1	64

```

/proc/cpuinfo cache data
cache size : 12288 KB

```

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Platform Notes (Continued)

From numactl --hardware

WARNING: a numactl 'node' might or might not correspond to a physical chip.

```
available: 1 nodes (0)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11
node 0 size: 128742 MB
node 0 free: 128257 MB
node distances:
node 0
0: 10
```

From /proc/meminfo

```
MemTotal: 131832256 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
```

From /etc/*release* /etc/*version*

```
os-release:
NAME="SLES"
VERSION="15-SP3"
VERSION_ID="15.3"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP3"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp3"
```

uname -a:

```
Linux localhost 5.3.18-57-default #1 SMP Wed Apr 28 10:54:41 UTC 2021 (ba3c2e9) x86_64
x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

```
CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store
Bypass disabled via prctl and
seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swaps
barriers and __user pointer
sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB:
conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected
```

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Platform Notes (Continued)

run-level 3 Mar 8 13:52

SPEC is set to: /home/cpu2017

Filesystem	Type	Size	Used	Avail	Use%	Mounted on
/dev/sda4	xfs	404G	46G	358G	12%	/home

From /sys/devices/virtual/dmi/id

```
Vendor:          HPE
Product:         ProLiant DL20 Gen10 Plus
Product Family: ProLiant
Serial:          SerNum.ACC
```

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:

4x Hynix HMAA4GU7AJR8N-XN 32 GB 2 rank 3200, configured at 2933

BIOS:

```
BIOS Vendor:      HPE
BIOS Version:     U60
BIOS Date:        01/13/2022
BIOS Revision:    1.54
Firmware Revision: 2.55
```

(End of data from sysinfo program)

Compiler Version Notes

=====
C | 500.perlbench_r(peak)
=====

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
=====

=====
C | 502.gcc_r(peak)
=====

Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
=====

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Compiler Version Notes (Continued)

```
=====
C          | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
          | 525.x264_r(base, peak) 557.xz_r(base, peak)
-----
```

```
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----
```

```
=====
C          | 500.perlbench_r(peak)
-----
```

```
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----
```

```
=====
C          | 502.gcc_r(peak)
-----
```

```
Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version
2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----
```

```
=====
C          | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
          | 525.x264_r(base, peak) 557.xz_r(base, peak)
-----
```

```
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----
```

```
=====
C          | 500.perlbench_r(peak)
-----
```

```
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
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Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----
```

```
=====
C          | 502.gcc_r(peak)
-----
```

```
Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version
```

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Compiler Version Notes (Continued)

2021.1 Build 20201113

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```

=====
C          | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
          | 525.x264_r(base, peak) 557.xz_r(base, peak)
=====

```

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

```

=====
C++       | 520.omnetpp_r(base, peak) 523.xalanbmk_r(base, peak)
          | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
=====

```

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

```

=====
Fortran   | 548.exchange2_r(base, peak)
=====

```

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000

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Base Compiler Invocation

C benchmarks:

icx

C++ benchmarks:

icpx

Fortran benchmarks:

ifort



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Base Portability Flags

```
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
```

Base Optimization Flags

C benchmarks:

```
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc
```

C++ benchmarks:

```
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc
```

Fortran benchmarks:

```
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-auto -mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc
```

Peak Compiler Invocation

C benchmarks (except as noted below):

icx

500.perlbench_r: icc

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Peak Compiler Invocation (Continued)

C++ benchmarks:

icpx

Fortran benchmarks:

ifort

Peak Portability Flags

```
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
```

Peak Optimization Flags

C benchmarks:

```
500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

502.gcc_r: -m32
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/ia32_lin
-std=gnu89 -Wl,-z,muldefs -fprofile-generate(pass 1)
-fprofile-use=default.profddata(pass 2) -xCORE-AVX512 -flto
-Ofast(pass 1) -O3 -ffast-math -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc32-5.0.1/lib -ljemalloc

505.mcf_r: basepeak = yes

525.x264_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto
-O3 -ffast-math -qopt-mem-layout-trans=4 -fno-alias
```

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Peak Optimization Flags (Continued)

525.x264_r (continued):

-mbranches-within-32B-boundaries

-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin

-lqkmalloc

557.xz_r: basepeak = yes

C++ benchmarks:

520.omnetpp_r: basepeak = yes

523.xalancbmk_r: basepeak = yes

531.deepsjeng_r: basepeak = yes

541.leela_r: basepeak = yes

Fortran benchmarks:

548.exchange2_r: basepeak = yes

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.0-ICX-revE.html>

http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.html

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.0-ICX-revE.xml>

http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml

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