SPEC CPU®2017 Floating Point Rate Result
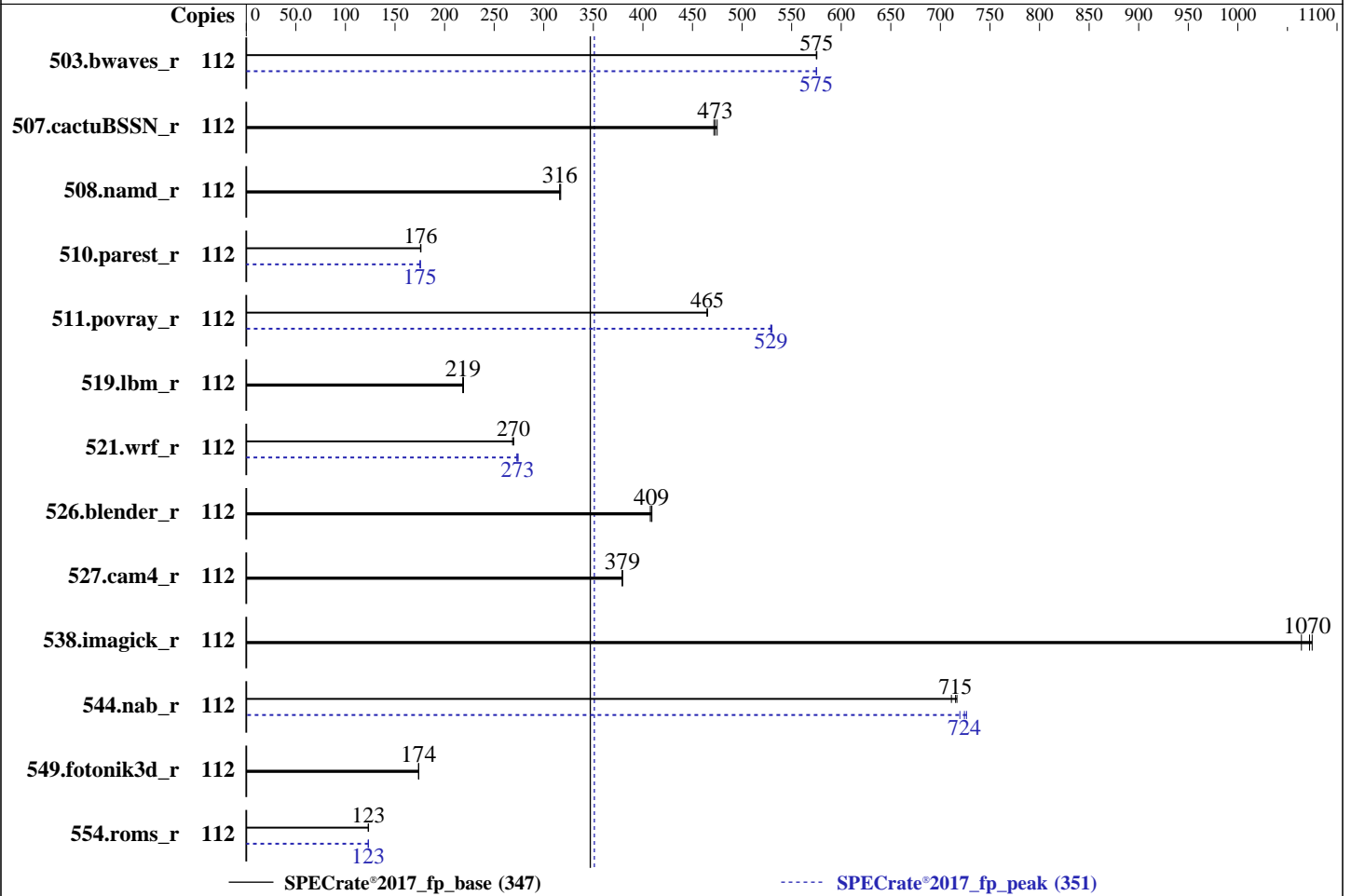
Copyright 2017-2021 Standard Performance Evaluation Corporation

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)

Tyrone Camarero SDI100C3R-212
(2.60 GHz, Intel Xeon Gold 6348)

$SPECrate®2017\_fp\_base = 347$

$SPECrate®2017\_fp\_peak = 351$

CPU2017 License: 006042	**Test Date:**	Jul-2021
Test Sponsor: Netweb Pte Ltd	**Hardware Availability:**	Apr-2021
Tested by: Tyrone Systems	**Software Availability:**	Jun-2021

Copies

Benchmark	Copies	base	peak
503.bwaves_r	112	575	575
507.cactuBSSN_r	112	473	
508.namd_r	112	316	
510.parest_r	112	176	175
511.povray_r	112	465	529
519.lbm_r	112	219	
521.wrf_r	112	270	273
526.blender_r	112	409	
527.cam4_r	112	379	
538.imagick_r	112	1070	
544.nab_r	112	715	724
549.fotonik3d_r	112	174	
554.roms_r	112	123	123

SPECrate®2017_fp_base (347)   SPECrate®2017_fp_peak (351)

Hardware

CPU Name: Intel Xeon Gold 6348
  Max MHz: 3500
  Nominal: 2600
Enabled: 56 cores, 2 chips, 2 threads/core
Orderable: 1,2 Chips
Cache L1: 32 KB I + 48 KB D on chip per core
  L2: 1.25 MB I+D on chip per core
  L3: 42 MB I+D on chip per chip
  Other: None
Memory: 256 GB (16 x 16 GB 1Rx4 PC4-3200AA-R)
Storage: 1 x 480 GB SATA SSD
Other: None

Software

OS: CentOS Linux release 8.4.2105
  Kernel 4.18.0-305.3.1.el8.x86_64
Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++
  Compiler Build 20201113 for Linux;
  Fortran: Version 2021.1 of Intel Fortran Compiler
  Classic Build 20201112 for Linux;
  C/C++: Version 2021.1 of Intel C/C++ Compiler
  Classic Build 20201112 for Linux
Parallel: No
Firmware: Version 1.1a released Jun-2021
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS set to prefer performance at the cost of
  additional power usage.

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)

Tyrone Camarero SDI100C3R-212
(2.60 GHz, Intel Xeon Gold 6348)

SPECrate®2017_fp_base = 347

SPECrate®2017_fp_peak = 351

CPU2017 License: 006042	**Test Date:** Jul-2021
Test Sponsor: Netweb Pte Ltd	**Hardware Availability:** Apr-2021
Tested by: Tyrone Systems	**Software Availability:** Jun-2021

Results Table

Benchmark	Base						Peak					
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	112	**1953**	**575**	1952	575	1954	575	112	1953	575	**1953**	**575**	1953	575
507.cactuBSSN_r	112	**300**	**473**	299	475	301	472	112	**300**	**473**	299	475	301	472
508.namd_r	112	**336**	**316**	336	317	337	316	112	**336**	**316**	336	317	337	316
510.parest_r	112	**1665**	**176**	1668	176	1664	176	112	1668	176	**1671**	**175**	1672	175
511.povray_r	112	**563**	**465**	563	465	562	465	112	494	529	**494**	**529**	493	530
519.lbm_r	112	**540**	**219**	541	218	539	219	112	**540**	**219**	541	218	539	219
521.wrf_r	112	934	269	**931**	**270**	930	270	112	915	274	919	273	**917**	**273**
526.blender_r	112	**418**	**409**	417	409	419	407	112	**418**	**409**	417	409	419	407
527.cam4_r	112	516	379	517	379	**516**	**379**	112	516	379	517	379	**516**	**379**
538.imagick_r	112	262	1060	259	1070	**260**	**1070**	112	262	1060	259	1070	**260**	**1070**
544.nab_r	112	265	711	**264**	**715**	263	717	112	**260**	**724**	262	720	260	726
549.fotonik3d_r	112	2510	174	**2510**	**174**	2511	174	112	2510	174	**2510**	**174**	2511	174
554.roms_r	112	1447	123	1443	123	**1445**	**123**	112	**1446**	**123**	1444	123	1447	123
SPECrate®2017_fp_base =		**347**										
SPECrate®2017_fp_peak =		**351**										

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"

General Notes

Binaries compiled locally by Netweb
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>   /proc/sys/vm/drop_caches

(Continued on next page)

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)

Tyrone Camarero SDI100C3R-212
(2.60 GHz, Intel Xeon Gold 6348)

SPECrate®2017_fp_base = 347

SPECrate®2017_fp_peak = 351

CPU2017 License: 006042	**Test Date:** Jul-2021
Test Sponsor: Netweb Pte Ltd	**Hardware Availability:** Apr-2021
Tested by: Tyrone Systems	**Software Availability:** Jun-2021

General Notes (Continued)

```
 runcpu command invoked through numactl i.e.:
 numactl --interleave=all runcpu <etc>
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

```
 jemalloc, a general purpose malloc implementation
 built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
 sources available from jemalloc.net or https://github.com/jemalloc/jemalloc/releases
```

Platform Notes

```
BIOS Settings:
Power Technology set to Custom
Power Performance Tuning set to BIOS Controls EPB
ENERGY_PERF_BIAS_CFG mode set to Performance
LLC Dead Line Alloc set to Disable

 Sysinfo program /home/cpu2017/bin/sysinfo
 Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
 running on localhost.localdomain Wed Aug 11 08:41:06 2021

 SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
    https://www.spec.org/cpu2017/Docs/config.html#sysinfo

 From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Gold 6348 CPU @ 2.60GHz
       2  "physical id"s (chips)
       112 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following
    excerpts from /proc/cpuinfo might not be reliable.  Use with caution.)
       cpu cores : 28
       siblings  : 56
       physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
       25 26 27
       physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
       25 26 27

 From lscpu from util-linux 2.32.1:
    Architecture:        x86_64
    CPU op-mode(s):      32-bit, 64-bit
    Byte Order:          Little Endian
```

(Continued on next page)

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)

Tyrone Camarero SDI100C3R-212
(2.60 GHz, Intel Xeon Gold 6348)

SPECrate®2017_fp_base = 347

SPECrate®2017_fp_peak = 351

CPU2017 License: 006042

Test Sponsor: Netweb Pte Ltd

Tested by: Tyrone Systems

Test Date: Jul-2021

Hardware Availability: Apr-2021

Software Availability: Jun-2021

Platform Notes (Continued)

```
          CPU(s):                112
          On-line CPU(s) list:   0-111
          Thread(s) per core:    2
          Core(s) per socket:    28
          Socket(s):             2
          NUMA node(s):          2
          Vendor ID:             GenuineIntel
          BIOS Vendor ID:        Intel(R) Corporation
          CPU family:            6
          Model:                 106
          Model name:            Intel(R) Xeon(R) Gold 6348 CPU @ 2.60GHz
          BIOS Model name:       Intel(R) Xeon(R) Gold 6348 CPU @ 2.60GHz
          Stepping:              6
          CPU MHz:               1927.832
          CPU max MHz:           3500.0000
          CPU min MHz:           800.0000
          BogoMIPS:              5200.00
          Virtualization:        VT-x
          L1d cache:             48K
          L1i cache:             32K
          L2 cache:              1280K
          L3 cache:              43008K
          NUMA node0 CPU(s):     0-27,56-83
          NUMA node1 CPU(s):     28-55,84-111
          Flags:                 fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
      pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
      lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
      aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
      xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
      avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single
      intel_ppin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority ept
      vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid cqm rdt_a
      avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha_ni
      avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
      cqm_mbm_local split_lock_detect wbnoinvd dtherm ida arat pln pts avx512vbmi umip pku
      ospke avx512_vbmi2 gfni vaes vpclmulqdq avx512_vnni avx512_bitalg tme
      avx512_vpopcntdq la57 rdpid fsrm md_clear pconfig flush_l1d arch_capabilities

 /proc/cpuinfo cache data
    cache size : 43008 KB

 From numactl --hardware
 WARNING: a numactl 'node' might or might not correspond to a physical chip.
   available: 2 nodes (0-1)
   node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
   56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83
   node 0 size: 128601 MB
```

(Continued on next page)

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)

Tyrone Camarero SDI100C3R-212
(2.60 GHz, Intel Xeon Gold 6348)

SPECrate®2017_fp_base = 347

SPECrate®2017_fp_peak = 351

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Test Date: Jul-2021
Hardware Availability: Apr-2021
Software Availability: Jun-2021

Platform Notes (Continued)

```
   node 0 free: 102301 MB
   node 1 cpus: 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52
   53 54 55 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100 101 102 103 104 105 106
   107 108 109 110 111
   node 1 size: 128972 MB
   node 1 free: 104329 MB
   node distances:
   node   0   1
     0:  10  20
     1:  20  10


From /proc/meminfo
   MemTotal:        263755836 kB
   HugePages_Total:         0
   Hugepagesize:         2048 kB


/sbin/tuned-adm active
     Current active profile: throughput-performance


/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has
   performance


From /etc/*release* /etc/*version*
   centos-release: CentOS Linux release 8.4.2105
   centos-release-upstream: Derived from Red Hat Enterprise Linux 8.4
   os-release:
      NAME="CentOS Linux"
      VERSION="8"
      ID="centos"
      ID_LIKE="rhel fedora"
      VERSION_ID="8"
      PLATFORM_ID="platform:el8"
      PRETTY_NAME="CentOS Linux 8"
      ANSI_COLOR="0;31"
   redhat-release: CentOS Linux release 8.4.2105
   system-release: CentOS Linux release 8.4.2105
   system-release-cpe: cpe:/o:centos:centos:8


uname -a:
   Linux localhost.localdomain 4.18.0-305.3.1.el8.x86_64 #1 SMP Tue Jun 1 16:14:33 UTC
   2021 x86_64 x86_64 x86_64 GNU/Linux


Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit):                    Not affected
CVE-2018-3620 (L1 Terminal Fault):                 Not affected
Microarchitectural Data Sampling:                  Not affected
```

(Continued on next page)

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)

Tyrone Camarero SDI100C3R-212
(2.60 GHz, Intel Xeon Gold 6348)

SPECrate®2017_fp_base = 347

SPECrate®2017_fp_peak = 351

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Test Date: Jul-2021
Hardware Availability: Apr-2021
Software Availability: Jun-2021

Platform Notes (Continued)

```
CVE-2017-5754 (Meltdown):                           Not affected
CVE-2018-3639 (Speculative Store Bypass):           Mitigation: Speculative Store
                                                    Bypass disabled via prctl and
                                                    seccomp
CVE-2017-5753 (Spectre variant 1):                  Mitigation: usercopy/swapgs
                                                    barriers and __user pointer
                                                    sanitization
CVE-2017-5715 (Spectre variant 2):                  Mitigation: Enhanced IBRS, IBPB:
                                                    conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort):            Not affected


run-level 3 Dec 31 19:08


SPEC is set to: /home/cpu2017
   Filesystem            Type  Size  Used Avail Use% Mounted on
   /dev/mapper/cl-home xfs   163G  108G   56G  67% /home


From /sys/devices/virtual/dmi/id
    Vendor:          Tyrone Systems
    Product:         Tyrone Camarero SDI100C3R-212
    Product Family:  SMC X12
    Serial:          123456789


Additional information from dmidecode 3.2 follows.  WARNING: Use caution when you
interpret this section. The 'dmidecode' program reads system data which is "intended to
allow hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  Memory:
    16x Samsung M393A2K40DB3-CWE 16 GB 1 rank 3200


BIOS:
   BIOS Vendor:      American Megatrends International, LLC.
   BIOS Version:     1.1a
   BIOS Date:        06/25/2021
   BIOS Revision:    5.22


(End of data from sysinfo program)
```

Compiler Version Notes

```
==============================================================================
C               | 519.lbm_r(base, peak) 538.imagick_r(base, peak)
                | 544.nab_r(base, peak)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
```

(Continued on next page)

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)

Tyrone Camarero SDI100C3R-212
(2.60 GHz, Intel Xeon Gold 6348)

SPECrate®2017_fp_base = 347

SPECrate®2017_fp_peak = 351

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Test Date: Jul-2021
Hardware Availability: Apr-2021
Software Availability: Jun-2021

Compiler Version Notes (Continued)

```
   Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C++                | 508.namd_r(base, peak) 510.parest_r(base, peak)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C++, C             | 511.povray_r(peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on
  Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
  64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C++, C             | 511.povray_r(base) 526.blender_r(base, peak)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C++, C             | 511.povray_r(peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on
  Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
  64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C++, C             | 511.povray_r(base) 526.blender_r(base, peak)
```

(Continued on next page)

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)

SPECrate®2017_fp_base = 347

Tyrone Camarero SDI100C3R-212
(2.60 GHz, Intel Xeon Gold 6348)

SPECrate®2017_fp_peak = 351

CPU2017 License: 006042

Test Sponsor: Netweb Pte Ltd

Tested by: Tyrone Systems

Test Date: Jul-2021

Hardware Availability: Apr-2021

Software Availability: Jun-2021

Compiler Version Notes (Continued)

```
--------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
--------------------------------------------------------------------------------


================================================================================
C++, C, Fortran | 507.cactuBSSN_r(base, peak)
--------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
  Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
--------------------------------------------------------------------------------


================================================================================
Fortran         | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
                | 554.roms_r(base, peak)
--------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
  Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
--------------------------------------------------------------------------------


================================================================================
Fortran, C      | 521.wrf_r(peak)
--------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
  Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
  64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
--------------------------------------------------------------------------------


================================================================================
Fortran, C      | 521.wrf_r(base) 527.cam4_r(base, peak)
--------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
```

(Continued on next page)

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)

SPECrate®2017_fp_base = 347

Tyrone Camarero SDI100C3R-212
(2.60 GHz, Intel Xeon Gold 6348)

SPECrate®2017_fp_peak = 351

CPU2017 License: 006042		**Test Date:**	Jul-2021
Test Sponsor: Netweb Pte Ltd		**Hardware Availability:**	Apr-2021
Tested by: Tyrone Systems		**Software Availability:**	Jun-2021

Compiler Version Notes (Continued)

```
  Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------


==============================================================================
Fortran, C     | 521.wrf_r(peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
  Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
  64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
Fortran, C     | 521.wrf_r(base) 527.cam4_r(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
  Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
```

Base Compiler Invocation

C benchmarks:
```
icx
```

C++ benchmarks:
```
icpx
```

Fortran benchmarks:
```
ifort
```

Benchmarks using both Fortran and C:
```
ifort icx
```

Benchmarks using both C and C++:
```
icpx icx
```

(Continued on next page)

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)

Tyrone Camarero SDI100C3R-212
(2.60 GHz, Intel Xeon Gold 6348)

SPECrate®2017_fp_base = 347

SPECrate®2017_fp_peak = 351

CPU2017 License: 006042

Test Sponsor: Netweb Pte Ltd

Tested by: Tyrone Systems

Test Date: Jul-2021

Hardware Availability: Apr-2021

Software Availability: Jun-2021

Base Compiler Invocation (Continued)

Benchmarks using Fortran, C, and C++:
```
icpx icx ifort
```

Base Portability Flags

503.bwaves_r: `-DSPEC_LP64`
507.cactuBSSN_r: `-DSPEC_LP64`
508.namd_r: `-DSPEC_LP64`
510.parest_r: `-DSPEC_LP64`
511.povray_r: `-DSPEC_LP64`
519.lbm_r: `-DSPEC_LP64`
521.wrf_r: `-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian`
526.blender_r: `-DSPEC_LP64 -DSPEC_LINUX -funsigned-char`
527.cam4_r: `-DSPEC_LP64 -DSPEC_CASE_FLAG`
538.imagick_r: `-DSPEC_LP64`
544.nab_r: `-DSPEC_LP64`
549.fotonik3d_r: `-DSPEC_LP64`
554.roms_r: `-DSPEC_LP64`

Base Optimization Flags

C benchmarks:
```
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc -L/usr/local/je5.0.1-64/lib
```

C++ benchmarks:
```
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc -L/usr/local/je5.0.1-64/lib
```

Fortran benchmarks:
```
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries -ljemalloc -L/usr/local/je5.0.1-64/lib
```

Benchmarks using both Fortran and C:
```
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
```

(Continued on next page)

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)

SPECrate®2017_fp_base = 347

Tyrone Camarero SDI100C3R-212
(2.60 GHz, Intel Xeon Gold 6348)

SPECrate®2017_fp_peak = 351

CPU2017 License: 006042	**Test Date:** Jul-2021
Test Sponsor: Netweb Pte Ltd	**Hardware Availability:** Apr-2021
Tested by: Tyrone Systems	**Software Availability:** Jun-2021

Base Optimization Flags (Continued)

Benchmarks using both Fortran and C (continued):
```
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/je5.0.1-64/lib
```

Benchmarks using both C and C++:
```
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc -L/usr/local/je5.0.1-64/lib
```

Benchmarks using Fortran, C, and C++:
```
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/je5.0.1-64/lib
```

Peak Compiler Invocation

C benchmarks:
```
icx
```

C++ benchmarks:
```
icpx
```

Fortran benchmarks:
```
ifort
```

Benchmarks using both Fortran and C:

521.wrf_r: `ifort icc`

527.cam4_r: `ifort icx`

Benchmarks using both C and C++:

511.povray_r: `icpc icc`

526.blender_r: `icpx icx`

Benchmarks using Fortran, C, and C++:
```
icpx icx ifort
```

Standard Performance Evaluation Corporation (info@spec.org)   https://www.spec.org/

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)

Tyrone Camarero SDI100C3R-212
(2.60 GHz, Intel Xeon Gold 6348)

SPECrate®2017_fp_base = 347

SPECrate®2017_fp_peak = 351

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Test Date: Jul-2021
Hardware Availability: Apr-2021
Software Availability: Jun-2021

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

519.lbm_r: basepeak = yes

538.imagick_r: basepeak = yes

544.nab_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto
-Ofast -qopt-mem-layout-trans=4
-fimf-accuracy-bits=14:sqrt
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/je5.0.1-64/lib

C++ benchmarks:

508.namd_r: basepeak = yes

510.parest_r: -w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-ljemalloc -L/usr/local/je5.0.1-64/lib

Fortran benchmarks:

503.bwaves_r: -w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs
-align array32byte -auto -mbranches-within-32B-boundaries
-ljemalloc -L/usr/local/je5.0.1-64/lib

549.fotonik3d_r: basepeak = yes

554.roms_r: Same as 503.bwaves_r

Benchmarks using both Fortran and C:

521.wrf_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries

(Continued on next page)

Standard Performance Evaluation Corporation (info@spec.org)   https://www.spec.org/

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)

Tyrone Camarero SDI100C3R-212
(2.60 GHz, Intel Xeon Gold 6348)

SPECrate®2017_fp_base = 347

SPECrate®2017_fp_peak = 351

CPU2017 License: 006042   **Test Date:** Jul-2021

Test Sponsor: Netweb Pte Ltd   **Hardware Availability:** Apr-2021

Tested by: Tyrone Systems   **Software Availability:** Jun-2021

Peak Optimization Flags (Continued)

521.wrf_r (continued):
```
-nostandard-realloc-lhs -align array32byte -auto
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

527.cam4_r: basepeak = yes

Benchmarks using both C and C++:

511.povray_r: `-prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3`
```
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

526.blender_r: basepeak = yes

Benchmarks using Fortran, C, and C++:

507.cactuBSSN_r: basepeak = yes

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.html
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revI.html

---

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revI.xml

---

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-08-11 08:41:06-0400.
Report generated on 2021-09-21 16:16:51 by CPU2017 PDF formatter v6442.
Originally published on 2021-09-21.