



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Dell Inc.

SPECrate®2017_int_base = 108

PowerEdge T440 (Intel Xeon Silver 4210, 2.20 GHz)

SPECrate®2017_int_peak = 112

CPU2017 License: 55

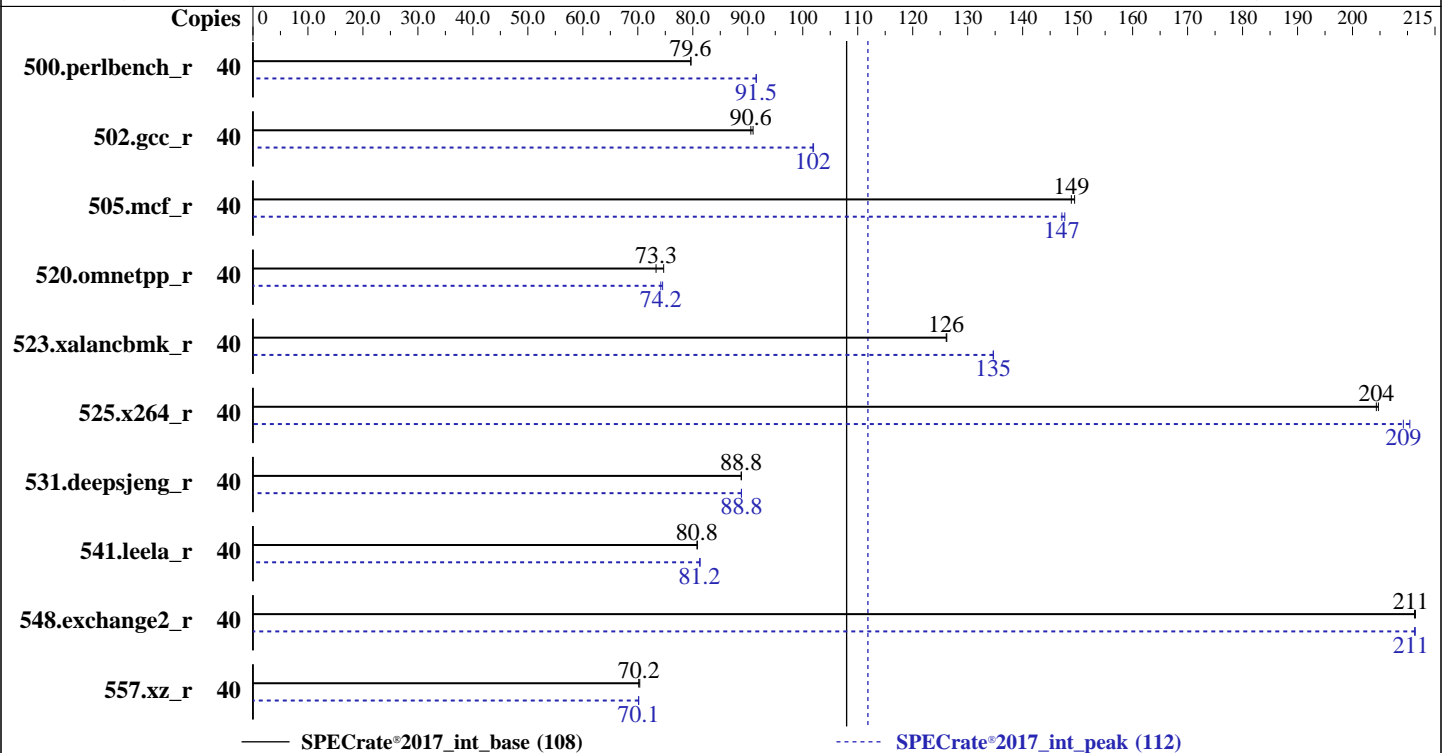
Test Date: Mar-2020

Test Sponsor: Dell Inc.

Hardware Availability: Dec-2019

Tested by: Dell Inc.

Software Availability: Jun-2019



Hardware

CPU Name: Intel Xeon Silver 4210
 Max MHz: 3200
 Nominal: 2200
 Enabled: 20 cores, 2 chips, 2 threads/core
 Orderable: 1,2 chips
 Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 13.75 MB I+D on chip per chip
 Other: None
 Memory: 384 GB (12 x 32 GB 2Rx8 PC4-2933V-R, running at 2666)
 Storage: 1 x 960 GB SATA SSD
 Other: None

Software

OS: SUSE Linux Enterprise Server 15 SP1
 kernel 4.12.14-195-default
 Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler Build 20190416 for Linux;
 Fortran: Version 19.0.4.227 of Intel Fortran Compiler Build 20190416 for Linux
 Parallel: No
 Firmware: Version 2.5.4 released Jan-2020
 File System: xfs
 System State: Run level 3 (multi-user)
 Base Pointers: 64-bit
 Peak Pointers: 32/64-bit
 Other: None
 jemalloc memory allocator V5.0.1
 Power Management: BIOS set to prefer performance at the cost of additional power usage.



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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
500.perlbench_r	40	799	79.7	800	79.6			40	695	91.6	696	91.5		
502.gcc_r	40	623	91.0	625	90.6			40	556	102	555	102		
505.mcf_r	40	433	149	434	149			40	438	148	439	147		
520.omnetpp_r	40	702	74.7	716	73.3			40	707	74.2	704	74.5		
523.xalancbmk_r	40	335	126	335	126			40	314	135	314	135		
525.x264_r	40	342	205	343	204			40	335	209	333	210		
531.deepsjeng_r	40	516	88.8	516	88.8			40	516	88.9	516	88.8		
541.leela_r	40	820	80.8	819	80.8			40	815	81.2	814	81.3		
548.exchange2_r	40	496	211	496	211			40	496	211	496	211		
557.xz_r	40	614	70.4	616	70.2			40	616	70.1	616	70.2		

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH =
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"
```

General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

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General Notes (Continued)

Transparent Huge Pages enabled by default
 Prior to runcpu invocation
 Filesystem page cache synced and cleared with:
`sync; echo 3> /proc/sys/vm/drop_caches`
 runcpu command invoked through numactl i.e.:
`numactl --interleave=all runcpu <etc>`
 jemalloc, a general purpose malloc implementation
 built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
 sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

Platform Notes

BIOS settings:
 Sub NUMA Cluster enabled
 Virtualization Technology disabled
 DCU Streamer Prefetcher disabled
 System Profile set to Custom
 CPU Performance set to Maximum Performance
 C States set to Autonomous
 C1E disabled
 Uncore Frequency set to Dynamic
 Energy Efficiency Policy set to Performance
 Memory Patrol Scrub disabled
 Logical Processor enabled
 CPU Interconnect Bus Link Power Management enabled
 PCI ASPM L1 Link Power Management enabled

Sysinfo program /home/cpu2017/bin/sysinfo
 Rev: r6365 of 2019-08-21 295195f888a3d7edble6e46a485a0011
 running on linux-g3ob Sun Mar 15 11:04:24 2020

SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

```

model name : Intel(R) Xeon(R) Silver 4210 CPU @ 2.20GHz
 2 "physical id"s (chips)
 40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 10
siblings : 20
physical 0: cores 0 1 2 3 4 8 9 10 11 12
physical 1: cores 0 1 2 3 4 8 9 10 11 12

```

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Platform Notes (Continued)

From lscpu:

```

Architecture:          x86_64
CPU op-mode(s):       32-bit, 64-bit
Byte Order:           Little Endian
Address sizes:        46 bits physical, 48 bits virtual
CPU(s):               40
On-line CPU(s) list: 0-39
Thread(s) per core:   2
Core(s) per socket:  10
Socket(s):            2
NUMA node(s):        2
Vendor ID:            GenuineIntel
CPU family:           6
Model:                85
Model name:           Intel(R) Xeon(R) Silver 4210 CPU @ 2.20GHz
Stepping:             6
CPU MHz:              2200.000
BogoMIPS:             4400.00
Virtualization:      VT-x
L1d cache:           32K
L1i cache:           32K
L2 cache:            1024K
L3 cache:            14080K
NUMA node0 CPU(s):   0,2,4,6,8,10,12,14,16,18,20,22,24,26,28,30,32,34,36,38
NUMA node1 CPU(s):   1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31,33,35,37,39
Flags:                fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx fl6c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
invpcid_single intel_ppin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi
flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm
cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd
avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
cqm_mbm_local dtherm ida arat pln pts pku ospke avx512_vnni md_clear flush_l1d
arch_capabilities

```

```

/proc/cpuinfo cache data
cache size : 14080 KB

```

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38
node 0 size: 192074 MB
node 0 free: 191643 MB

```

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Platform Notes (Continued)

```
node 1 cpus: 1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31 33 35 37 39
node 1 size: 193501 MB
node 1 free: 192949 MB
node distances:
node 0 1
0: 10 21
1: 21 10
```

From /proc/meminfo

```
MemTotal: 394829660 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
```

From /etc/*release* /etc/*version*

```
os-release:
NAME="SLES"
VERSION="15-SP1"
VERSION_ID="15.1"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP1"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp1"
```

uname -a:

```
Linux linux-g3ob 4.12.14-195-default #1 SMP Tue May 7 10:55:11 UTC 2019 (8fba516)
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

```
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled
via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional,
RSB filling
```

run-level 3 Mar 15 11:01 last=5

SPEC is set to: /home/cpu2017

```
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 xfs 440G 52G 389G 12% /
```

From /sys/devices/virtual/dmi/id

BIOS: Dell Inc. 2.5.4 01/14/2020

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Platform Notes (Continued)

Vendor: Dell Inc.
Product: PowerEdge T440
Product Family: PowerEdge
Serial: FBLH613

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:

4x 00AD00B300AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933
8x 00AD063200AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933
4x Not Specified Not Specified

(End of data from sysinfo program)

Compiler Version Notes

=====
C | 502.gcc_r(peak)

Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

=====
C | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
525.x264_r(base, peak) 557.xz_r(base, peak)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
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C | 502.gcc_r(peak)

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Compiler Version Notes (Continued)

```
-----
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----
```

```
=====
C++      | 523.xalancbmk_r(peak)
-----
```

```
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----
```

```
=====
C++      | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
          | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
-----
```

```
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----
```

```
=====
C++      | 523.xalancbmk_r(peak)
-----
```

```
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----
```

```
=====
C++      | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
          | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
-----
```

```
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----
```

```
=====
Fortran  | 548.exchange2_r(base, peak)
-----
```

```
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----
```



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Base Compiler Invocation

C benchmarks:

```
icc -m64 -std=c11
```

C++ benchmarks:

```
icpc -m64
```

Fortran benchmarks:

```
ifort -m64
```

Base Portability Flags

```
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
```

Base Optimization Flags

C benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```

C++ benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```

Fortran benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```




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Peak Compiler Invocation

C benchmarks (except as noted below):

```
icc -m64 -std=c11
```

```
502.gcc_r: icc -m32 -std=c11 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin
```

C++ benchmarks (except as noted below):

```
icpc -m64
```

```
523.xalancbmk_r: icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin
```

Fortran benchmarks:

```
ifort -m64
```

Peak Portability Flags

```
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
```

```
502.gcc_r: -D_FILE_OFFSET_BITS=64
```

```
505.mcf_r: -DSPEC_LP64
```

```
520.omnetpp_r: -DSPEC_LP64
```

```
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
```

```
525.x264_r: -DSPEC_LP64
```

```
531.deepsjeng_r: -DSPEC_LP64
```

```
541.leela_r: -DSPEC_LP64
```

```
548.exchange2_r: -DSPEC_LP64
```

```
557.xz_r: -DSPEC_LP64
```

Peak Optimization Flags

C benchmarks:

```
500.perlbench_r: -w1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
```

```
-xCORE-AVX2 -O3 -no-prec-div -qopt-mem-layout-trans=4
```

```
-fno-strict-overflow
```

```
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
```

```
-lqkmalloc
```

```
502.gcc_r: -w1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
```

```
-xCORE-AVX2 -O3 -no-prec-div -qopt-mem-layout-trans=4
```

```
-L/usr/local/je5.0.1-32/lib -ljemalloc
```

```
505.mcf_r: -w1,-z,muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div
```

```
-qopt-mem-layout-trans=4
```

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Peak Optimization Flags (Continued)

505.mcf_r (continued):

```
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmallocc
```

525.x264_r: -Wl, -z, muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div

```
-qopt-mem-layout-trans=4 -fno-alias
```

```
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmallocc
```

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

520.omnetpp_r: -Wl, -z, muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div

```
-qopt-mem-layout-trans=4
```

```
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmallocc
```

523.xalancbmk_r: -Wl, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo

```
-xCORE-AVX2 -O3 -no-prec-div -qopt-mem-layout-trans=4
```

```
-L/usr/local/je5.0.1-32/lib -ljemallocc
```

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:

```
-Wl, -z, muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div
```

```
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
```

```
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmallocc
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.html>

<http://www.spec.org/cpu2017/flags/Dell-Platform-Flags-PowerEdge-revE9.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.xml>

<http://www.spec.org/cpu2017/flags/Dell-Platform-Flags-PowerEdge-revE9.xml>



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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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