



SPEC® CPU2017 Integer Rate Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 6144
3.50 GHz)

SPECrate2017_int_base = 116

SPECrate2017_int_peak = 122

CPU2017 License: 9019

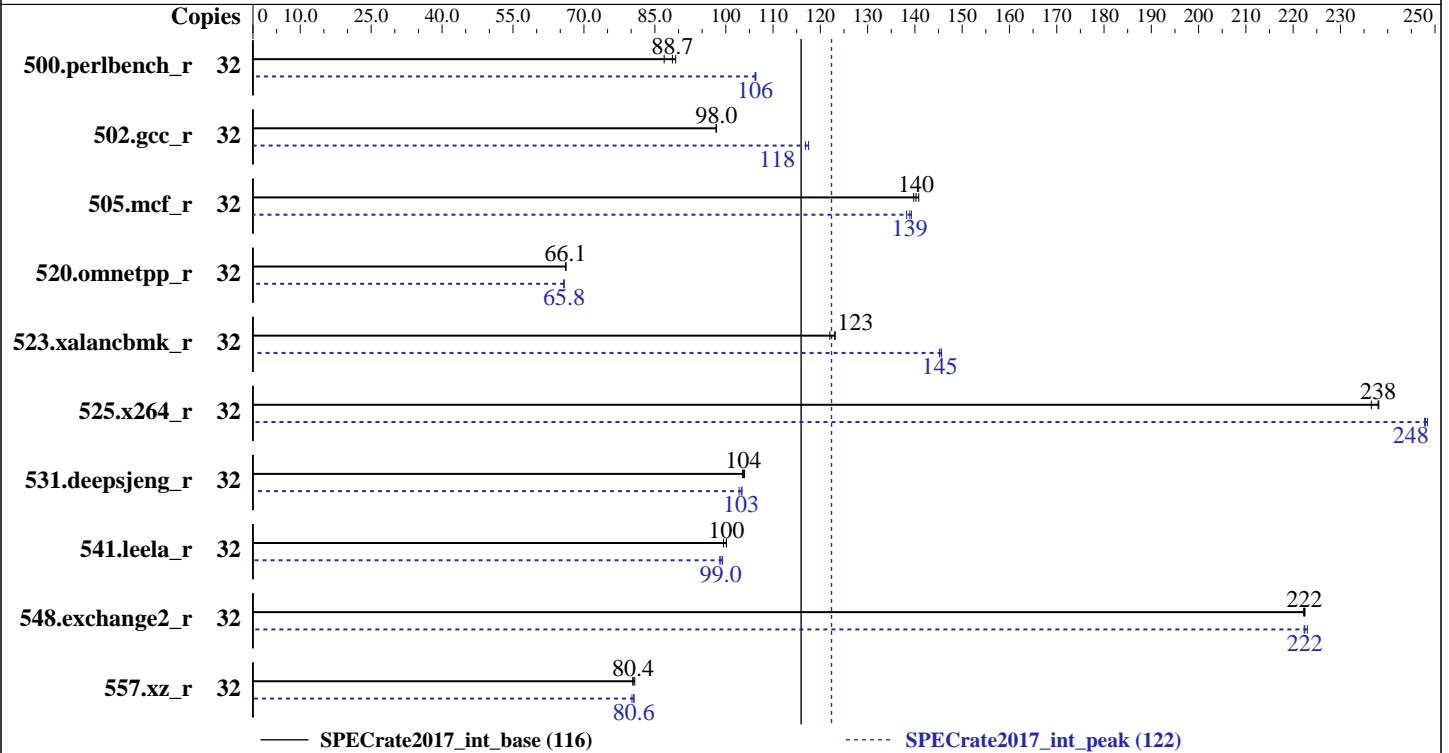
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Dec-2018

Hardware Availability: Aug-2017

Software Availability: Nov-2018



Hardware

CPU Name: Intel Xeon Gold 6144
 Max MHz.: 4200
 Nominal: 3500
 Enabled: 16 cores, 2 chips, 2 threads/core
 Orderable: 1,2 Chips
 Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 24.75 MB I+D on chip per chip
 Other: None
 Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2666V-R)
 Storage: 1 x 240 GB M.2 SATA SSD
 Other: None

Software

OS: SUSE Linux Enterprise Server 12 SP3 (x86_64)
 4.4.120-94.17-default
 Compiler: C/C++: Version 19.0.1.144 of Intel C/C++
 Compiler for Linux;
 Fortran: Version 19.0.1.144 of Intel Fortran
 Compiler for Linux
 Parallel: No
 Firmware: Version 4.0.1 released Oct-2018
 File System: xfs
 System State: Run level 3 (multi-user)
 Base Pointers: 64-bit
 Peak Pointers: 32/64-bit
 Other: jemalloc memory allocator V5.0.1



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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
500.perlbench_r	32	<u>574</u>	<u>88.7</u>	586	87.0	570	89.4	32	<u>480</u>	<u>106</u>	479	106	480	106
502.gcc_r	32	<u>462</u>	<u>98.0</u>	463	98.0	462	98.1	32	386	118	<u>386</u>	<u>118</u>	388	117
505.mcf_r	32	<u>369</u>	<u>140</u>	367	141	370	140	32	374	138	371	139	<u>372</u>	<u>139</u>
520.omnetpp_r	32	635	66.1	634	66.2	<u>635</u>	<u>66.1</u>	32	638	65.8	<u>638</u>	<u>65.8</u>	639	65.7
523.xalancbmk_r	32	277	122	<u>275</u>	<u>123</u>	274	123	32	233	145	232	146	<u>233</u>	<u>145</u>
525.x264_r	32	<u>235</u>	<u>238</u>	237	237	235	238	32	226	248	226	248	<u>226</u>	<u>248</u>
531.deepsjeng_r	32	353	104	354	104	<u>353</u>	<u>104</u>	32	354	103	<u>355</u>	<u>103</u>	357	103
541.leela_r	32	529	100	<u>529</u>	<u>100</u>	532	99.5	32	<u>535</u>	<u>99.0</u>	537	98.7	534	99.3
548.exchange2_r	32	377	222	<u>377</u>	<u>222</u>	377	222	32	377	222	376	223	<u>377</u>	<u>222</u>
557.xz_r	32	428	80.7	430	80.3	<u>430</u>	<u>80.4</u>	32	<u>429</u>	<u>80.6</u>	431	80.2	429	80.6

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:

LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation

Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

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General Notes (Continued)

jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-4dlf Thu Dec 20 06:24:59 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6144 CPU @ 3.50GHz
2 "physical id"s (chips)
32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 16
physical 0: cores 0 2 3 9 16 19 26 27
physical 1: cores 0 2 3 9 16 19 26 27

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 32
On-line CPU(s) list: 0-31
Thread(s) per core: 2
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6144 CPU @ 3.50GHz

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Platform Notes (Continued)

```
Stepping: 4
CPU MHz: 4054.112
CPU max MHz: 4200.0000
CPU min MHz: 1200.0000
BogoMIPS: 6983.60
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0,1,3,4,16,17,19,20
NUMA node1 CPU(s): 2,5-7,18,21-23
NUMA node2 CPU(s): 8,9,11,12,24,25,27,28
NUMA node3 CPU(s): 10,13-15,26,29-31
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmpperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts
dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt rsb_ctxsw spec_ctrl stibp
retpoline kaiser tpr_shadow vmmi flexpriority ept vpid fsgsbase tsc_adjust bml1 hle
avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt
clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc pku
ospke
```

```
/proc/cpuinfo cache data
cache size : 25344 KB
```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```
available: 4 nodes (0-3)
node 0 cpus: 0 1 3 4 16 17 19 20
node 0 size: 192100 MB
node 0 free: 190519 MB
node 1 cpus: 2 5 6 7 18 21 22 23
node 1 size: 193531 MB
node 1 free: 192131 MB
node 2 cpus: 8 9 11 12 24 25 27 28
node 2 size: 193531 MB
node 2 free: 192137 MB
node 3 cpus: 10 13 14 15 26 29 30 31
node 3 size: 193529 MB
node 3 free: 192135 MB
node distances:
node 0 1 2 3
0: 10 11 21 21
```

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Platform Notes (Continued)

```

1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

```

From /proc/meminfo

```

MemTotal:      791237296 kB
HugePages_Total:      0
Hugepagesize:    2048 kB

```

From /etc/*release* /etc/*version*

SuSE-release:

```

SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 3

```

```

# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.

```

os-release:

```

NAME="SLES"
VERSION="12-SP3"
VERSION_ID="12.3"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP3"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp3"

```

uname -a:

```

Linux linux-4dlf 4.4.120-94.17-default #1 SMP Wed Mar 14 17:23:00 UTC 2018 (cf3a7bb)
x86_64 x86_64 x86_64 GNU/Linux

```

Kernel self-reported vulnerability status:

```

CVE-2017-5754 (Meltdown):      Mitigation: PTI
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: IBRS+IBPB

```

run-level 3 Dec 20 00:08

SPEC is set to: /home/cpu2017

```

Filesystem      Type      Size      Used Avail Use% Mounted on
/dev/sdc2        xfs       220G      33G  188G  15% /

```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

```

BIOS Cisco Systems, Inc. C220M5.4.0.1.139.1003182107 10/03/2018
Memory:

```

(Continued on next page)



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Platform Notes (Continued)

7x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666
17x 0xCE00 M393A4K40CB2-CTD 32 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

=====
CC 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
525.x264_r(base, peak) 557.xz_r(base, peak)
=====

icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
=====

=====
CC 500.perlbench_r(peak) 502.gcc_r(peak)
=====

icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
=====

=====
CXXC 520.omnetpp_r(base) 523.xalanbmk_r(base) 531.deepsjeng_r(base)
541.leela_r(base)
=====

icpc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
=====

=====
CXXC 520.omnetpp_r(peak) 523.xalanbmk_r(peak) 531.deepsjeng_r(peak)
541.leela_r(peak)
=====

icpc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
=====

=====
FC 548.exchange2_r(base, peak)
=====

ifort (IFORT) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
=====



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Base Compiler Invocation

C benchmarks:

```
icc -m64 -std=c11
```

C++ benchmarks:

```
icpc -m64
```

Fortran benchmarks:

```
ifort -m64
```

Base Portability Flags

```
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64  
502.gcc_r: -DSPEC_LP64  
505.mcf_r: -DSPEC_LP64  
520.omnetpp_r: -DSPEC_LP64  
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX  
525.x264_r: -DSPEC_LP64  
531.deepsjeng_r: -DSPEC_LP64  
541.leela_r: -DSPEC_LP64  
548.exchange2_r: -DSPEC_LP64  
557.xz_r: -DSPEC_LP64
```

Base Optimization Flags

C benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

C++ benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

Fortran benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte  
-L/home/cpu2017/je5.0.1-64/ -ljemalloc
```



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Peak Compiler Invocation

C benchmarks (except as noted below):

```
icc -m64 -std=c11
```

```
502.gcc_r: icc -m32 -std=c11 -L/opt/intel/lib/ia32
```

C++ benchmarks (except as noted below):

```
icpc -m64
```

```
523.xalancbmk_r: icpc -m32 -L/opt/intel/lib/ia32
```

Fortran benchmarks:

```
ifort -m64
```

Peak Portability Flags

```
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
```

```
502.gcc_r: -D_FILE_OFFSET_BITS=64
```

```
505.mcf_r: -DSPEC_LP64
```

```
520.omnetpp_r: -DSPEC_LP64
```

```
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
```

```
525.x264_r: -DSPEC_LP64
```

```
531.deepsjeng_r: -DSPEC_LP64
```

```
541.leela_r: -DSPEC_LP64
```

```
548.exchange2_r: -DSPEC_LP64
```

```
557.xz_r: -DSPEC_LP64
```

Peak Optimization Flags

C benchmarks:

```
500.perlbench_r: -w1, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-fno-strict-overflow -L/home/cpu2017/je5.0.1-64/  
-ljemalloc
```

```
502.gcc_r: -w1, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-L/home/cpu2017/je5.0.1-32/ -ljemalloc
```

```
505.mcf_r: -w1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/  
-ljemalloc
```

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Peak Optimization Flags (Continued)

525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -fno-alias
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

520.omnetpp_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

523.xalancbmk_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-L/home/cpu2017/je5.0.1-32/ -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml>

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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