



# SPEC® CPU2017 Integer Rate Result

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## Supermicro

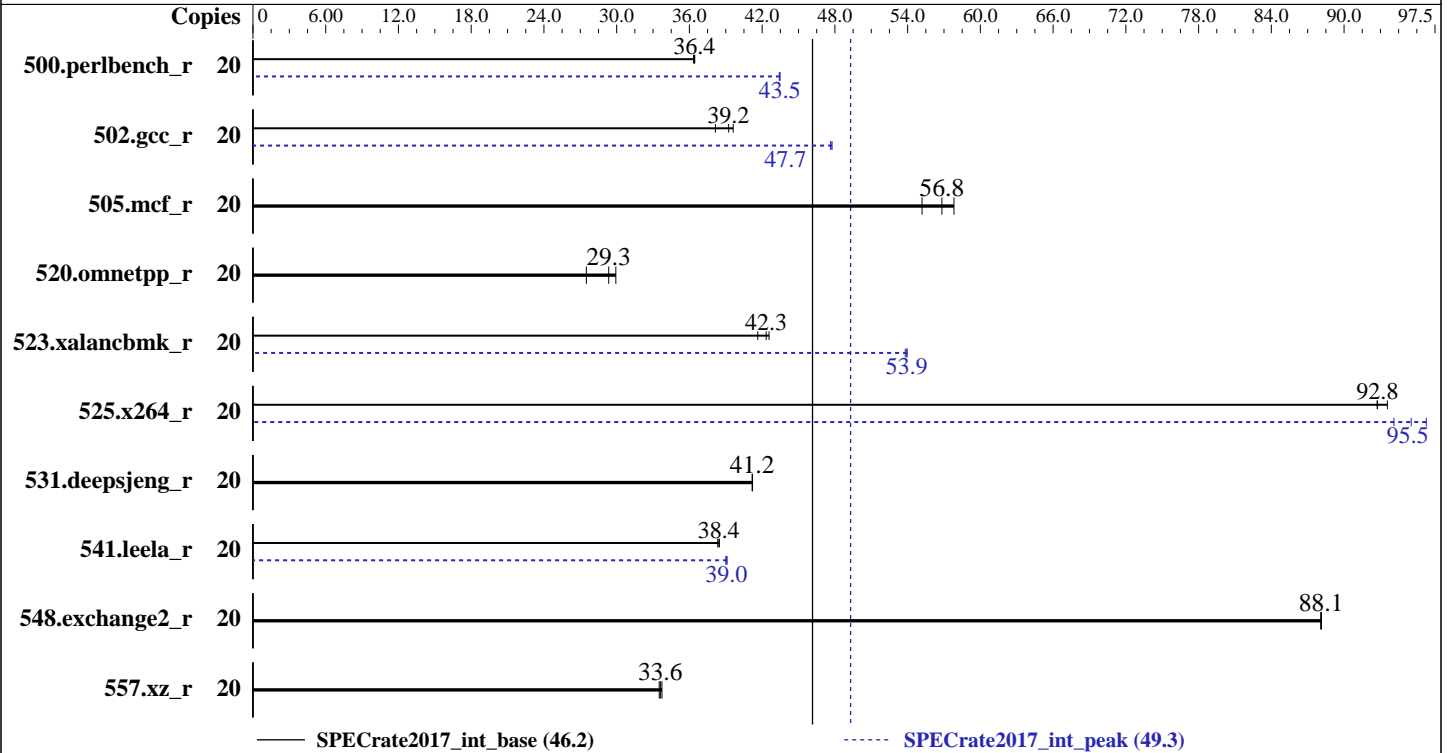
SuperStorage 5029P-E1CTR12L (X11SPH-nCTF, Intel Xeon Silver 4114)

SPECrate2017\_int\_base = 46.2

SPECrate2017\_int\_peak = 49.3

CPU2017 License: 001176  
Test Sponsor: Supermicro  
Tested by: Supermicro

Test Date: Jun-2018  
Hardware Availability: Jul-2017  
Software Availability: Mar-2018



### Hardware

CPU Name: Intel Xeon Silver 4114  
Max MHz.: 3000  
Nominal: 2200  
Enabled: 10 cores, 1 chip, 2 threads/core  
Orderable: 1 chip  
Cache L1: 32 KB I + 32 KB D on chip per core  
L2: 1 MB I+D on chip per core  
L3: 13.75 MB I+D on chip per chip  
Other: None  
Memory: 192 GB (6 x 32 GB 2Rx4 PC4-2666V-R, running at 2400)  
Storage: 1 x 2 TB NVMe SSD  
Other: None

### Software

OS: SUSE Linux Enterprise Server 12 SP3 (x86\_64)  
Kernel 4.4.114-94.11-default  
Compiler: C/C++: Version 18.0.2.199 of Intel C/C++ Compiler for Linux;  
Fortran: Version 18.0.2.199 of Intel Fortran Compiler for Linux  
Parallel: No  
Firmware: Supermicro BIOS version 2.1 released Jun-2018  
File System: xfs  
System State: Run level 3 (multi-user)  
Base Pointers: 64-bit  
Peak Pointers: 32/64-bit  
Other: jemalloc memory allocator library V5.0.1



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## Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
500.perlbench_r	20	876	36.3	874	36.4	<b>874</b>	<b>36.4</b>	20	733	43.4	732	43.5	<b>733</b>	<b>43.5</b>
502.gcc_r	20	742	38.1	<b>722</b>	<b>39.2</b>	715	39.6	20	593	47.8	<b>594</b>	<b>47.7</b>	594	47.6
505.mcf_r	20	559	57.8	586	55.2	<b>569</b>	<b>56.8</b>	20	559	57.8	586	55.2	<b>569</b>	<b>56.8</b>
520.omnetpp_r	20	954	27.5	<b>894</b>	<b>29.3</b>	877	29.9	20	954	27.5	<b>894</b>	<b>29.3</b>	877	29.9
523.xalancbmk_r	20	507	41.6	<b>499</b>	<b>42.3</b>	496	42.6	20	<b>392</b>	<b>53.9</b>	393	53.8	391	54.0
525.x264_r	20	374	93.6	<b>378</b>	<b>92.8</b>	378	92.7	20	362	96.8	372	94.1	<b>367</b>	<b>95.5</b>
531.deepsjeng_r	20	556	41.2	<b>556</b>	<b>41.2</b>	556	41.2	20	556	41.2	<b>556</b>	<b>41.2</b>	556	41.2
541.leela_r	20	<b>862</b>	<b>38.4</b>	864	38.3	861	38.5	20	<b>848</b>	<b>39.0</b>	847	39.1	849	39.0
548.exchange2_r	20	<b>595</b>	<b>88.1</b>	595	88.1	595	88.1	20	<b>595</b>	<b>88.1</b>	595	88.1	595	88.1
557.xz_r	20	645	33.5	640	33.7	<b>643</b>	<b>33.6</b>	20	645	33.5	640	33.7	<b>643</b>	<b>33.6</b>

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## General Notes

Environment variables set by runcpu before the start of the run:

LD\_LIBRARY\_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

Binaries compiled on a system with 1x Intel Core i7-6700K CPU + 32GB RAM

memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

runcpu command invoked through numactl i.e.:

```
numactl --interleave=all runcpu <etc>
```

jemalloc: jemalloc, a general purpose malloc implementation;

jemalloc: built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5;

jemalloc: sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

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## General Notes (Continued)

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

## Platform Notes

### BIOS Settings:

LLC prefetch = Enable  
Power Technology = Custom  
Power Performance Tuning = BIOS Controls EPB  
ENERGY\_PERF\_BIAS\_CFG mode = Maximum Performance  
Hardware P-state = Out of Band Mode  
SNC = Enable  
XPT Prefetch = Enable  
Stale AtoS = Enable  
LLC dead line alloc = Disable  
IMC Interleaving = 1-way Interleave  
SDDC Plus One = Disable  
ADDDC Sparing = Disable  
Patrol Scrub = Disable  
Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f  
running on linux-liai Thu Jun 21 16:58:16 2018

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see  
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

### From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Silver 4114 CPU @ 2.20GHz
 1 "physical id"s (chips)
 20 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 10
  siblings  : 20
  physical 0: cores 0 1 2 3 4 8 9 10 11 12
```

### From lscpu:

```
Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Byte Order:            Little Endian
CPU(s):                 20
```

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### Platform Notes (Continued)

```

On-line CPU(s) list:    0-19
Thread(s) per core:    2
Core(s) per socket:    10
Socket(s):              1
NUMA node(s):          1
Vendor ID:              GenuineIntel
CPU family:             6
Model:                  85
Model name:             Intel(R) Xeon(R) Silver 4114 CPU @ 2.20GHz
Stepping:               4
CPU MHz:                2199.986
BogoMIPS:               4399.97
Virtualization:         VT-x
L1d cache:              32K
L1i cache:              32K
L2 cache:               1024K
L3 cache:               14080K
NUMA node0 CPU(s):     0-19
Flags:                  fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts
dtherm hwp_epp intel_pt rsb_ctxsw spec_ctrl retpoline kaiser tpr_shadow vnmi
flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm
cqm mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl
xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc pku ospke

```

```

/proc/cpuinfo cache data
cache size : 14080 KB

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```

available: 1 nodes (0)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
node 0 size: 192824 MB
node 0 free: 192031 MB
node distances:
node    0
0:     10

```

```

From /proc/meminfo
MemTotal:      197452140 kB
HugePages_Total:      0
Hugepagesize:    2048 kB

```

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## Platform Notes (Continued)

```

/usr/bin/lsb_release -d
    SUSE Linux Enterprise Server 12 SP3

From /etc/*release* /etc/*version*
SuSE-release:
    SUSE Linux Enterprise Server 12 (x86_64)
    VERSION = 12
    PATCHLEVEL = 3
    # This file is deprecated and will be removed in a future service pack or release.
    # Please check /etc/os-release for details about this release.
os-release:
    NAME="SLES"
    VERSION="12-SP3"
    VERSION_ID="12.3"
    PRETTY_NAME="SUSE Linux Enterprise Server 12 SP3"
    ID="sles"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:12:sp3"

uname -a:
    Linux linux-liai 4.4.114-94.11-default #1 SMP Thu Feb 1 19:28:26 UTC 2018 (4309ff9)
    x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jun 21 16:57

SPEC is set to: /home/cpu2017
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/nvme0n1p4  xfs   1.8T   56G  1.8T   4% /home

Additional information from dmidecode follows.  WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
BIOS American Megatrends Inc. 2.1 06/11/2018
Memory:
    2x NO DIMM NO DIMM
    6x Samsung M393A4K40CB2-CTD 32 GB 2 rank 2666, configured at 2400

(End of data from sysinfo program)

```

## Compiler Version Notes

```

=====
CC 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base) 525.x264_r(base)
    557.xz_r(base)
=====

```

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### Compiler Version Notes (Continued)

icc (ICC) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====  
CC 500.perlbench\_r(peak) 502.gcc\_r(peak) 505.mcf\_r(peak) 525.x264\_r(peak)  
557.xz\_r(peak)

icc (ICC) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====  
CXXC 520.omnetpp\_r(base) 523.xalancbmk\_r(base) 531.deepsjeng\_r(base)  
541.leela\_r(base)

icpc (ICC) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====  
CXXC 520.omnetpp\_r(peak) 523.xalancbmk\_r(peak) 531.deepsjeng\_r(peak)  
541.leela\_r(peak)

icpc (ICC) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====  
FC 548.exchange2\_r(base)

ifort (IFORT) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====  
FC 548.exchange2\_r(peak)

ifort (IFORT) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

### Base Compiler Invocation

C benchmarks:  
icc -m64 -std=c11

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## Base Compiler Invocation (Continued)

C++ benchmarks:

```
icpc -m64
```

Fortran benchmarks:

```
ifort -m64
```

## Base Portability Flags

```
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64  
502.gcc_r: -DSPEC_LP64  
505.mcf_r: -DSPEC_LP64  
520.omnetpp_r: -DSPEC_LP64  
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX  
525.x264_r: -DSPEC_LP64  
531.deepsjeng_r: -DSPEC_LP64  
541.leela_r: -DSPEC_LP64  
548.exchange2_r: -DSPEC_LP64  
557.xz_r: -DSPEC_LP64
```

## Base Optimization Flags

C benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc
```

C++ benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc
```

Fortran benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs  
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

## Peak Compiler Invocation

C benchmarks (except as noted below):

```
icc -m64 -std=c11
```

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## Peak Compiler Invocation (Continued)

```
502.gcc_r: icc -m32 -std=c11 -L/home/prasadj/specdev/IC18u2_Internal/lin_18_0_20180210/compiler/lib/ia32_lin
```

C++ benchmarks (except as noted below):

```
icpc -m64
```

```
523.xalancbmk_r: icpc -m32 -L/home/prasadj/specdev/IC18u2_Internal/lin_18_0_20180210/compiler/lib/ia32_lin
```

Fortran benchmarks:

```
ifort -m64
```

## Peak Portability Flags

```
500.perlbenc_r: -DSPEC_LP64 -DSPEC_LINUX_X64  
502.gcc_r: -D_FILE_OFFSET_BITS=64  
505.mcf_r: -DSPEC_LP64  
520.omnetpp_r: -DSPEC_LP64  
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX  
525.x264_r: -DSPEC_LP64  
531.deepsjeng_r: -DSPEC_LP64  
541.leela_r: -DSPEC_LP64  
548.exchange2_r: -DSPEC_LP64  
557.xz_r: -DSPEC_LP64
```

## Peak Optimization Flags

C benchmarks:

```
500.perlbenc_r: -w1, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-fno-strict-overflow -L/usr/local/je5.0.1-64/lib  
-ljemalloc
```

```
502.gcc_r: -w1, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-L/usr/local/je5.0.1-32/lib -ljemalloc
```

```
505.mcf_r: basepeak = yes
```

```
525.x264_r: -w1, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
```

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## Peak Optimization Flags (Continued)

525.x264\_r (continued):

```
-fno-alias -L/usr/local/je5.0.1-64/lib -ljemalloc
```

557.xz\_r: basepeak = yes

C++ benchmarks:

520.omnetpp\_r: basepeak = yes

```
523.xalancbmk_r: -w1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-L/usr/local/je5.0.1-32/lib -ljemalloc
```

531.deepsjeng\_r: basepeak = yes

```
541.leela_r: -w1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

Fortran benchmarks:

548.exchange2\_r: basepeak = yes

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2017-12-21.html>

<http://www.spec.org/cpu2017/flags/Supermicro-Platform-Settings-V1.2-SKL-revD.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2017-12-21.xml>

<http://www.spec.org/cpu2017/flags/Supermicro-Platform-Settings-V1.2-SKL-revD.xml>

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For questions about this result, please contact the tester. For other inquiries, please contact [info@spec.org](mailto:info@spec.org).

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