



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

SPECrate®2017_int_base = 460

SPECrate®2017_int_peak = 490

CPU2017 License: 9019

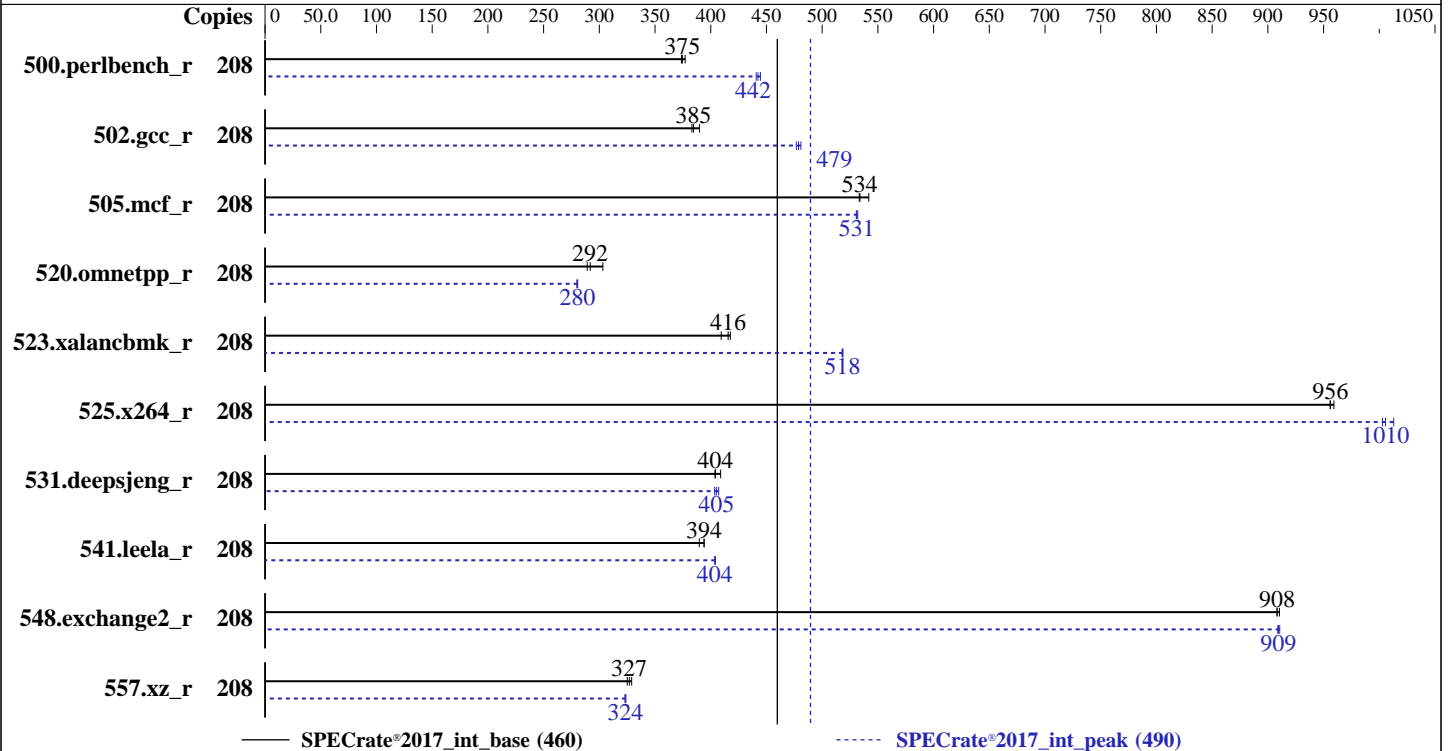
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: May-2018

Hardware Availability: Aug-2017

Software Availability: Mar-2018



Hardware

CPU Name: Intel Xeon Platinum 8164
 Max MHz: 3700
 Nominal: 2000
 Enabled: 104 cores, 4 chips, 2 threads/core
 Orderable: 2,4 Chips
 Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 35.75 MB I+D on chip per chip
 Other: None
 Memory: 768 GB (48 x 16 GB 2Rx4 PC4-2666V-R)
 Storage: 1 x 600 GB SAS HDD, 10K RPM
 Other: None

Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.103-92.56-default
 Compiler: C/C++: Version 18.0.2.199 of Intel C/C++ Compiler for Linux;
 Fortran: Version 18.0.2.199 of Intel Fortran Compiler for Linux
 Parallel: No
 Firmware: Version 3.2.3c released Mar-2018
 File System: xfs
 System State: Run level 3 (multi-user)
 Base Pointers: 64-bit
 Peak Pointers: 32/64-bit
 Other: jemalloc: jemalloc memory allocator library V5.0.1;
 Power Management: --



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

SPECrate®2017_int_base = 460

SPECrate®2017_int_peak = 490

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: May-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
500.perlbench_r	208	878	377	884	375	886	374	208	745	445	749	442	751	441
502.gcc_r	208	769	383	756	390	766	385	208	615	479	618	477	612	481
505.mcf_r	208	620	542	630	534	630	533	208	632	532	633	531	633	531
520.omnetpp_r	208	900	303	935	292	944	289	208	973	281	975	280	974	280
523.xalancbmk_r	208	526	418	537	409	528	416	208	423	519	424	518	424	518
525.x264_r	208	380	959	381	956	381	956	208	363	1000	362	1010	360	1010
531.deepsjeng_r	208	583	409	590	404	590	404	208	586	407	589	405	591	403
541.leela_r	208	884	390	874	394	874	394	208	852	404	853	404	853	404
548.exchange2_r	208	599	910	600	908	600	908	208	600	909	599	909	598	911
557.xz_r	208	683	329	687	327	691	325	208	694	324	696	323	694	324

SPECrate®2017_int_base = **460**

SPECrate®2017_int_peak = **490**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:

LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

(Continued on next page)



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

SPECrate®2017_int_base = 460

SPECrate®2017_int_peak = 490

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: May-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

General Notes (Continued)

jemalloc: configured and built at default for 32bit (i686) and 64bit (x86_64) targets;
jemalloc: built with the RedHat Enterprise 7.4, and the system compiler gcc 4.8.5;
jemalloc: sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-xy4f Sat May 19 01:31:53 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see <https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Platinum 8164 CPU @ 2.00GHz
4 "physical id"s (chips)
208 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 26
siblings : 52
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 22 24 25 26 27 28 29
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 22 24 25 26 27 28 29
physical 2: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 22 24 25 26 27 28 29
physical 3: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 22 24 25 26 27 28 29

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 208

(Continued on next page)



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

SPECrate®2017_int_base = 460

SPECrate®2017_int_peak = 490

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: May-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Platform Notes (Continued)

```

On-line CPU(s) list:    0-207
Thread(s) per core:    2
Core(s) per socket:    26
Socket(s):              4
NUMA node(s):          8
Vendor ID:              GenuineIntel
CPU family:             6
Model:                  85
Model name:             Intel(R) Xeon(R) Platinum 8164 CPU @ 2.00GHz
Stepping:               4
CPU MHz:                1245.090
CPU max MHz:            3700.0000
CPU min MHz:            1000.0000
BogoMIPS:               4000.01
Virtualization:         VT-x
L1d cache:              32K
L1i cache:              32K
L2 cache:               1024K
L3 cache:               36608K
NUMA node0 CPU(s):     0-3,7-9,13-15,20-22,104-107,111-113,117-119,124-126
NUMA node1 CPU(s):     4-6,10-12,16-19,23-25,108-110,114-116,120-123,127-129
NUMA node2 CPU(s):     26-29,33-35,39-41,46-48,130-133,137-139,143-145,150-152
NUMA node3 CPU(s):     30-32,36-38,42-45,49-51,134-136,140-142,146-149,153-155
NUMA node4 CPU(s):     52-55,59-61,65-67,72-74,156-159,163-165,169-171,176-178
NUMA node5 CPU(s):     56-58,62-64,68-71,75-77,160-162,166-168,172-175,179-181
NUMA node6 CPU(s):     78-81,85-87,91-93,98-100,182-185,189-191,195-197,202-204
NUMA node7 CPU(s):     82-84,88-90,94-97,101-103,186-188,192-194,198-201,205-207
Flags:                  fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmpperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts
dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt spec_ctrl kaiser tpr_shadow
vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid
rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw
avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc

```

```
/proc/cpuinfo cache data
cache size : 36608 KB
```

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 8 nodes (0-7)
node 0 cpus: 0 1 2 3 7 8 9 13 14 15 20 21 22 104 105 106 107 111 112 113 117 118 119
124 125 126
node 0 size: 95327 MB

```

(Continued on next page)



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

SPECrate®2017_int_base = 460

SPECrate®2017_int_peak = 490

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: May-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Platform Notes (Continued)

```

node 0 free: 95161 MB
node 1 cpus: 4 5 6 10 11 12 16 17 18 19 23 24 25 108 109 110 114 115 116 120 121 122
123 127 128 129
node 1 size: 96760 MB
node 1 free: 96564 MB
node 2 cpus: 26 27 28 29 33 34 35 39 40 41 46 47 48 130 131 132 133 137 138 139 143 144
145 150 151 152
node 2 size: 96760 MB
node 2 free: 96487 MB
node 3 cpus: 30 31 32 36 37 38 42 43 44 45 49 50 51 134 135 136 140 141 142 146 147 148
149 153 154 155
node 3 size: 96760 MB
node 3 free: 96546 MB
node 4 cpus: 52 53 54 55 59 60 61 65 66 67 72 73 74 156 157 158 159 163 164 165 169 170
171 176 177 178
node 4 size: 96760 MB
node 4 free: 96592 MB
node 5 cpus: 56 57 58 62 63 64 68 69 70 71 75 76 77 160 161 162 166 167 168 172 173 174
175 179 180 181
node 5 size: 96760 MB
node 5 free: 96607 MB
node 6 cpus: 78 79 80 81 85 86 87 91 92 93 98 99 100 182 183 184 185 189 190 191 195
196 197 202 203 204
node 6 size: 96760 MB
node 6 free: 96614 MB
node 7 cpus: 82 83 84 88 89 90 94 95 96 97 101 102 103 186 187 188 192 193 194 198 199
200 201 205 206 207
node 7 size: 96758 MB
node 7 free: 96619 MB
node distances:
node  0  1  2  3  4  5  6  7
0: 10 11 21 21 21 21 21 21
1: 11 10 21 21 21 21 21 21
2: 21 21 10 11 21 21 21 21
3: 21 21 11 10 21 21 21 21
4: 21 21 21 21 10 11 21 21
5: 21 21 21 21 11 10 21 21
6: 21 21 21 21 21 21 10 11
7: 21 21 21 21 21 21 11 10

```

```

From /proc/meminfo
MemTotal: 791191608 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

```

```

From /etc/*release* /etc/*version*
SuSE-release:

```

(Continued on next page)



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

SPECrate®2017_int_base = 460

SPECrate®2017_int_peak = 490

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: May-2018

Hardware Availability: Aug-2017

Software Availability: Mar-2018

Platform Notes (Continued)

SUSE Linux Enterprise Server 12 (x86_64)

VERSION = 12

PATCHLEVEL = 2

This file is deprecated and will be removed in a future service pack or release.

Please check /etc/os-release for details about this release.

os-release:

NAME="SLES"

VERSION="12-SP2"

VERSION_ID="12.2"

PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"

ID="sles"

ANSI_COLOR="0;32"

CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:

Linux linux-xy4f 4.4.103-92.56-default #1 SMP Wed Dec 27 16:24:31 UTC 2017 (2fd2155)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 4 04:57

SPEC is set to: /home/cpu2017

Filesystem	Type	Size	Used	Avail	Use%	Mounted on
/dev/sda1	xf	224G	68G	156G	31%	/

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B480M5.3.2.3c.0.0307181316 03/07/2018

Memory:

48x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

```

=====
C          | 500.perlbench_r(base, peak) 502.gcc_r(base, peak) 505.mcf_r(base,
          | peak) 525.x264_r(base, peak) 557.xz_r(base, peak)
=====

```

icc (ICC) 18.0.2 20180210

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

```

=====
C++       | 520.omnetpp_r(base, peak) 523.xalanbmk_r(base, peak)
=====

```

(Continued on next page)



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

SPECrate®2017_int_base = 460

SPECrate®2017_int_peak = 490

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: May-2018

Hardware Availability: Aug-2017

Software Availability: Mar-2018

Compiler Version Notes (Continued)

| 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)

icpc (ICC) 18.0.2 20180210

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====
Fortran | 548.exchange2_r(base, peak)

ifort (IFORT) 18.0.2 20180210

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:

icc -m64 -std=c11

C++ benchmarks:

icpc -m64

Fortran benchmarks:

ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64

502.gcc_r: -DSPEC_LP64

505.mcf_r: -DSPEC_LP64

520.omnetpp_r: -DSPEC_LP64

523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX

525.x264_r: -DSPEC_LP64

531.deepsjeng_r: -DSPEC_LP64

541.leela_r: -DSPEC_LP64

548.exchange2_r: -DSPEC_LP64

557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div

(Continued on next page)



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

SPECrate®2017_int_base = 460

SPECrate®2017_int_peak = 490

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: May-2018

Hardware Availability: Aug-2017

Software Availability: Mar-2018

Base Optimization Flags (Continued)

C benchmarks (continued):

```
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

C++ benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
```

```
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

Fortran benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
```

```
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
```

```
-L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

Peak Compiler Invocation

C benchmarks (except as noted below):

```
icc -m64 -std=c11
```

```
502.gcc_r: icc -m32 -std=c11 -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
```

C++ benchmarks (except as noted below):

```
icpc -m64
```

```
523.xalancbmk_r: icpc -m32 -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
```

Fortran benchmarks:

```
ifort -m64
```

Peak Portability Flags

```
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
```

```
502.gcc_r: -D_FILE_OFFSET_BITS=64
```

```
505.mcf_r: -DSPEC_LP64
```

```
520.omnetpp_r: -DSPEC_LP64
```

```
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
```

```
525.x264_r: -DSPEC_LP64
```

```
531.deepsjeng_r: -DSPEC_LP64
```

```
541.leela_r: -DSPEC_LP64
```

```
548.exchange2_r: -DSPEC_LP64
```

```
557.xz_r: -DSPEC_LP64
```




SPEC CPU®2017 Integer Rate Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8164,
2.00 GHz)

SPECrate®2017_int_base = 460

SPECrate®2017_int_peak = 490

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: May-2018

Hardware Availability: Aug-2017

Software Availability: Mar-2018

Peak Optimization Flags

C benchmarks:

```
500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-fno-strict-overflow -L/home/cpu2017/je5.0.1-64/  
-ljemalloc
```

```
502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-L/home/cpu2017/je5.0.1-32/ -ljemalloc
```

```
505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/  
-ljemalloc
```

```
525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -fno-alias  
-L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

```
520.omnetpp_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

```
523.xalancbmk_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-L/home/cpu2017/je5.0.1-32/ -ljemalloc
```

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte  
-L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2018-06-13.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html>



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

SPECrate®2017_int_base = 460

SPECrate®2017_int_peak = 490

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: May-2018

Hardware Availability: Aug-2017

Software Availability: Mar-2018

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2018-06-13.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml>

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2018-05-19 01:31:52-0400.

Report generated on 2019-12-13 17:52:44 by CPU2017 PDF formatter v6255.

Originally published on 2018-06-12.