



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8158, 3.00GHz)

SPECrate®2017_int_base = 154

SPECrate®2017_int_peak = 163

CPU2017 License: 9019

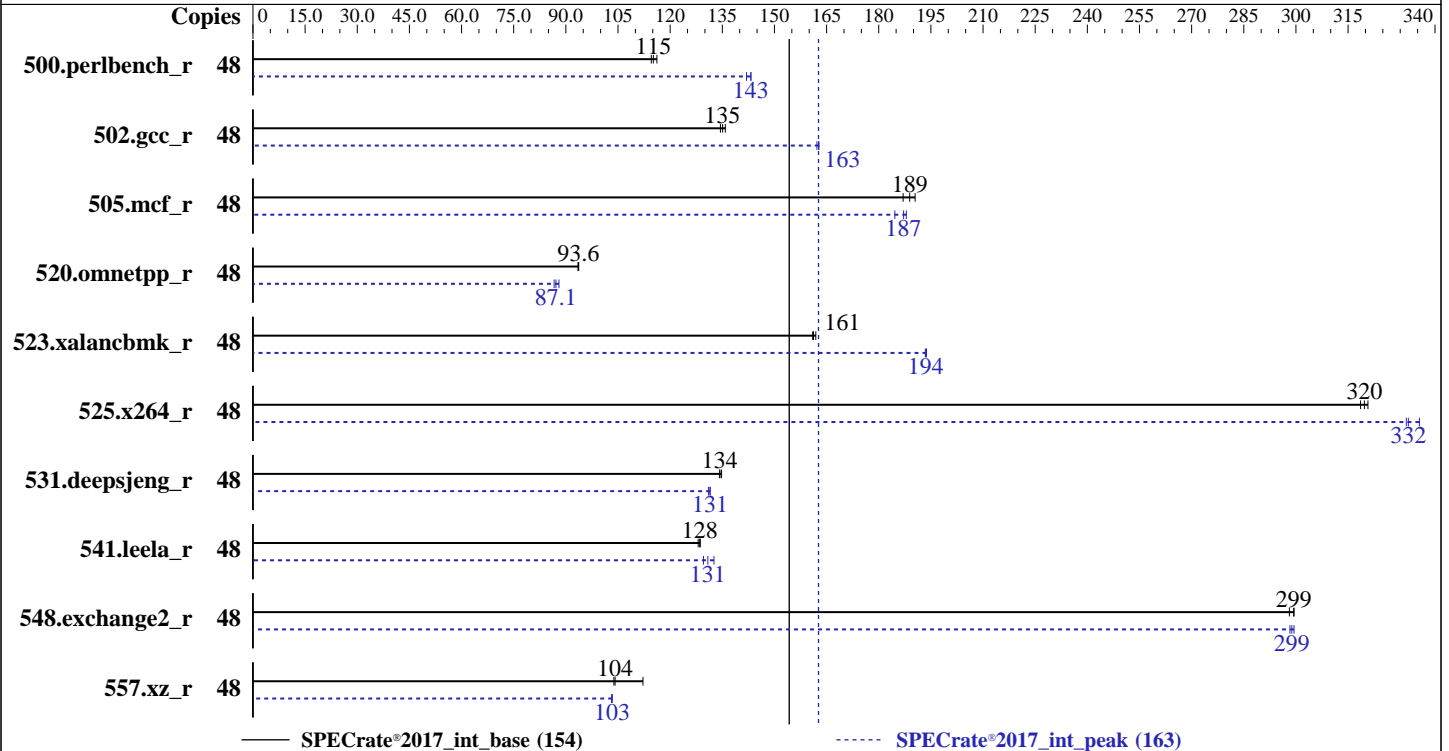
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Oct-2017

Hardware Availability: Aug-2017

Software Availability: Sep-2017



Hardware

CPU Name: Intel Xeon Platinum 8158
 Max MHz: 3700
 Nominal: 3000
 Enabled: 24 cores, 2 chips, 2 threads/core
 Orderable: 1,2 Chips
 Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 24.75 MB I+D on chip per chip
 Other: None
 Memory: 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)
 Storage: 1 x 1 TB SAS HDD, 7.2K RPM
 Other: None

Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default
 Compiler: C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux;
 Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux
 Parallel: No
 Firmware: Version 3.2.1d released Jul-2017
 File System: xfs
 System State: Run level 3 (multi-user)
 Base Pointers: 64-bit
 Peak Pointers: 32/64-bit
 Other: jemalloc: jemalloc memory allocator library V5.0.1;
 jemalloc: configured and built at default for 32bit (i686) and 64bit (x86_64) targets;
 jemalloc: built with the RedHat Enterprise 7.4, and the system compiler gcc 4.8.5;
 jemalloc: sources available from jemalloc.net or releases
 Power Management: --



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8158, 3.00GHz)

SPECrate®2017_int_base = 154

SPECrate®2017_int_peak = 163

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
500.perlbench_r	48	667	115	664	115	658	116	48	534	143	538	142	534	143
502.gcc_r	48	500	136	503	135	505	134	48	418	163	419	162	418	163
505.mcf_r	48	407	190	415	187	411	189	48	420	185	413	188	414	187
520.omnetpp_r	48	674	93.5	673	93.6	672	93.7	48	715	88.0	727	86.6	723	87.1
523.xalancbmk_r	48	313	162	314	161	315	161	48	262	194	262	193	262	194
525.x264_r	48	263	320	262	321	264	319	48	253	332	251	336	253	332
531.deepsjeng_r	48	408	135	410	134	410	134	48	418	132	420	131	418	131
541.leela_r	48	619	128	621	128	618	129	48	613	130	608	131	599	133
548.exchange2_r	48	420	299	420	299	422	298	48	421	299	422	298	420	299
557.xz_r	48	462	112	498	104	499	104	48	502	103	502	103	502	103

SPECrate®2017_int_base = **154**

SPECrate®2017_int_peak = **163**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The config file option 'submit' was used.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:

LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM

memory using Redhat Enterprise Linux 7.4

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

jemalloc, a general purpose malloc implementation

built with the RedHat Enterprise 7.4, and the system compiler gcc 4.8.5

sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Enabled

CPU performance set to Enterprise

(Continued on next page)



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8158, 3.00GHz)

SPECrate®2017_int_base = 154

SPECrate®2017_int_peak = 163

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Oct-2017

Hardware Availability: Aug-2017

Software Availability: Sep-2017

Platform Notes (Continued)

Power Performance Tuning set to OS
 SNC set to Enabled
 IMC Interleaving set to 1-way Interleave
 Patrol Scrub set to Disabled
 Sysinfo program /home/cpu2017/bin/sysinfo
 Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
 running on linux-uezu Sat Oct 14 08:04:10 2017

SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

```
From /proc/cpuinfo
model name      : Intel(R) Xeon(R) Platinum 8158 CPU @ 3.00GHz
 2 "physical id"s (chips)
 48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores      : 12
siblings       : 24
physical 0:    cores 0 1 2 3 4 9 10 16 18 19 25 26
physical 1:    cores 0 1 3 9 10 16 18 19 24 25 26 27
```

```
From lscpu:
Architecture:      x86_64
CPU op-mode(s):    32-bit, 64-bit
Byte Order:        Little Endian
CPU(s):            48
On-line CPU(s) list: 0-47
Thread(s) per core: 2
Core(s) per socket: 12
Socket(s):         2
NUMA node(s):     4
Vendor ID:         GenuineIntel
CPU family:        6
Model:             85
Model name:        Intel(R) Xeon(R) Platinum 8158 CPU @ 3.00GHz
Stepping:         4
CPU MHz:           2096.015
CPU max MHz:       3700.0000
CPU min MHz:       1200.0000
BogoMIPS:          6000.01
Virtualization:    VT-x
L1d cache:         32K
L1i cache:         32K
L2 cache:          1024K
L3 cache:          25344K
```

(Continued on next page)



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8158, 3.00GHz)

SPECrate®2017_int_base = 154

SPECrate®2017_int_peak = 163

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Oct-2017

Hardware Availability: Aug-2017

Software Availability: Sep-2017

Platform Notes (Continued)

```

NUMA node0 CPU(s):      0-2,5,7,10,24-26,29,31,34
NUMA node1 CPU(s):      3,4,6,8,9,11,27,28,30,32,33,35
NUMA node2 CPU(s):      12,13,15,17,20,21,36,37,39,41,44,45
NUMA node3 CPU(s):      14,16,18,19,22,23,38,40,42,43,46,47
Flags:                   fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmpperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb pln pts dtherm hwp
hwp_act_window hwp_epp hwp_pkg_req intel_pt tpr_shadow vnmi flexpriority ept vpid
fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f
avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec
xgetbv1 cqm_llc cqm_occup_llc

```

```

/proc/cpuinfo cache data
cache size : 25344 KB

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```

available: 4 nodes (0-3)
node 0 cpus: 0 1 2 5 7 10 24 25 26 29 31 34
node 0 size: 95320 MB
node 0 free: 92162 MB
node 1 cpus: 3 4 6 8 9 11 27 28 30 32 33 35
node 1 size: 96753 MB
node 1 free: 93724 MB
node 2 cpus: 12 13 15 17 20 21 36 37 39 41 44 45
node 2 size: 96753 MB
node 2 free: 93725 MB
node 3 cpus: 14 16 18 19 22 23 38 40 42 43 46 47
node 3 size: 96750 MB
node 3 free: 93257 MB
node distances:
node  0  1  2  3
 0:  10  11  21  21
 1:  11  10  21  21
 2:  21  21  10  11
 3:  21  21  11  10

```

```

From /proc/meminfo
MemTotal:      394831816 kB
HugePages_Total:      0
Hugepagesize:    2048 kB

```

```

From /etc/*release* /etc/*version*
SuSE-release:

```

(Continued on next page)



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8158, 3.00GHz)

SPECrate®2017_int_base = 154

SPECrate®2017_int_peak = 163

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Platform Notes (Continued)

```
SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.
```

```
os-release:
NAME="SLES"
VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"
```

```
uname -a:
Linux linux-uezu 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
x86_64 x86_64 x86_64 GNU/Linux
```

```
run-level 3 Jan 8 17:00
```

```
SPEC is set to: /home/cpu2017
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sda1       xfs   894G  108G  787G  13% /
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

```
BIOS Cisco Systems, Inc. B200M5.3.2.1d.5.0727171353 07/27/2017
Memory:
24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666
```

(End of data from sysinfo program)

Compiler Version Notes

```
=====
C          | 500.perlbench_r(base, peak) 502.gcc_r(base, peak) 505.mcf_r(base,
          | peak) 525.x264_r(base, peak) 557.xz_r(base, peak)
-----
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
-----
C++       | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak)
=====
```

(Continued on next page)



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8158, 3.00GHz)

SPECrate®2017_int_base = 154

SPECrate®2017_int_peak = 163

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Compiler Version Notes (Continued)

| 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)

icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

=====
Fortran | 548.exchange2_r(base, peak)

ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div

(Continued on next page)



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8158, 3.00GHz)

SPECrate®2017_int_base = 154

SPECrate®2017_int_peak = 163

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Oct-2017

Hardware Availability: Aug-2017

Software Availability: Sep-2017

Base Optimization Flags (Continued)

C benchmarks (continued):

```
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc
```

C++ benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc
```

Fortran benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte  
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

Base Other Flags

C benchmarks:

```
-m64 -std=c11
```

C++ benchmarks:

```
-m64
```

Fortran benchmarks:

```
-m64
```

Peak Compiler Invocation

C benchmarks:

```
icc
```

C++ benchmarks:

```
icpc
```

Fortran benchmarks:

```
ifort
```

Peak Portability Flags

```
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
```

```
502.gcc_r: -D_FILE_OFFSET_BITS=64
```

```
505.mcf_r: -DSPEC_LP64
```

(Continued on next page)



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8158, 3.00GHz)

SPECrate®2017_int_base = 154

SPECrate®2017_int_peak = 163

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Oct-2017

Hardware Availability: Aug-2017

Software Availability: Sep-2017

Peak Portability Flags (Continued)

```
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
```

Peak Optimization Flags

C benchmarks:

```
500.perlbench_r: -w1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-fno-strict-overflow -L/usr/local/je5.0.1-64/lib
-ljemalloc
```

```
502.gcc_r: -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
-w1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-L/usr/local/je5.0.1-32/lib -ljemalloc
```

```
505.mcf_r: -w1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib
-ljemalloc
```

```
525.x264_r: -w1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -fno-alias
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

```
520.omnetpp_r: -w1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

```
523.xalancbmk_r: -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
-w1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-L/usr/local/je5.0.1-32/lib -ljemalloc
```

(Continued on next page)



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8158, 3.00GHz)

SPECrate®2017_int_base = 154

SPECrate®2017_int_peak = 163

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Oct-2017

Hardware Availability: Aug-2017

Software Availability: Sep-2017

Peak Optimization Flags (Continued)

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte  
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

Peak Other Flags

C benchmarks (except as noted below):

```
-m64 -std=c11
```

502.gcc_r: -m32 -std=c11

C++ benchmarks (except as noted below):

```
-m64
```

523.xalancbmk_r: -m32

Fortran benchmarks:

```
-m64
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml>

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2017-10-14 08:04:10-0400.

Report generated on 2020-09-03 16:49:46 by CPU2017 PDF formatter v6255.

Originally published on 2017-10-31.