



SPEC® CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M3 (Intel Xeon E5-2630L v2, 2.40 GHz)

SPECint®2006 = 43.4

SPECint_base2006 = 41.2

CPU2006 license: 9019

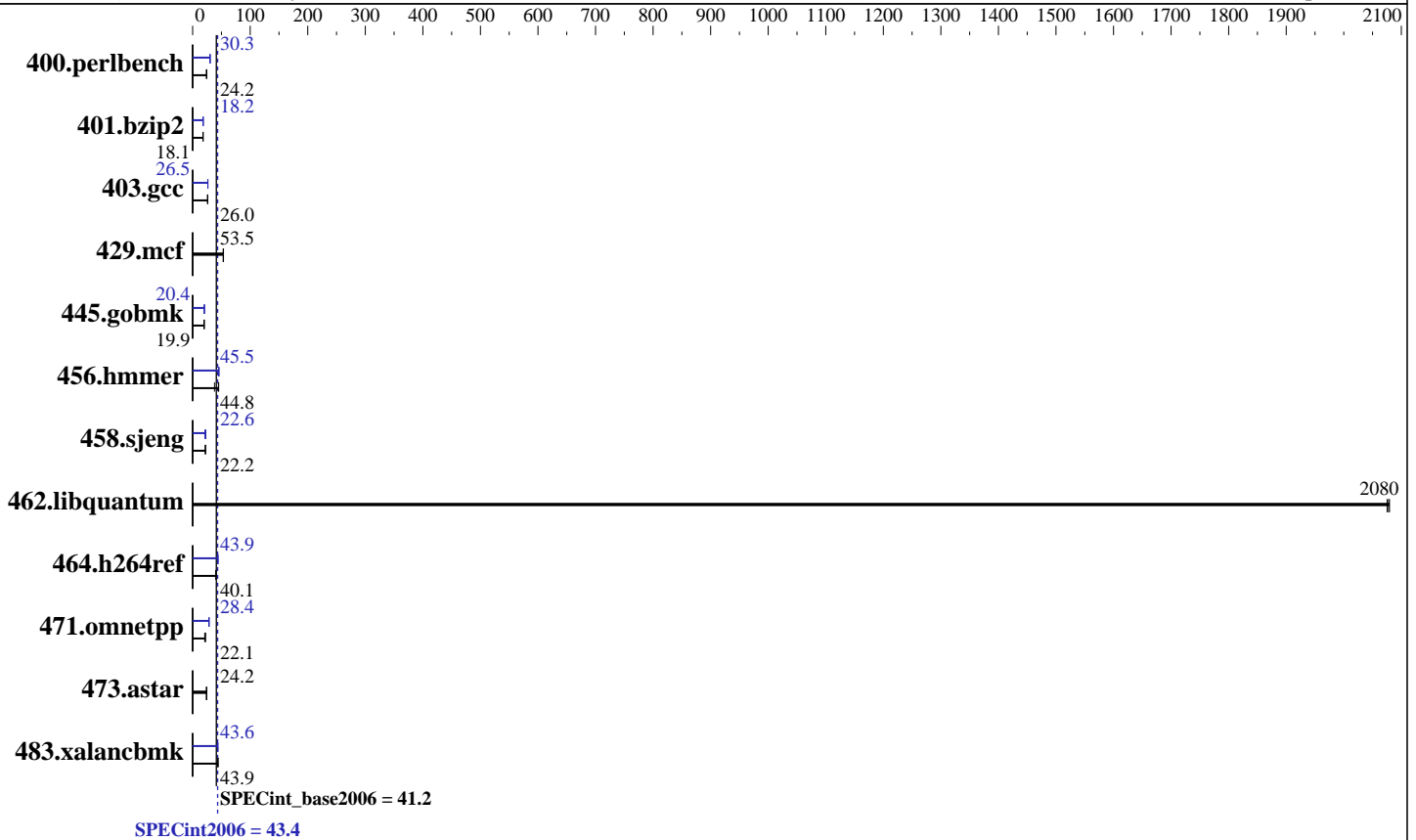
Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Dec-2013

Hardware Availability: Dec-2013

Software Availability: Sep-2013



Hardware

CPU Name: Intel Xeon E5-2630L v2
CPU Characteristics: Intel Turbo Boost Technology up to 2.80 GHz
CPU MHz: 2400
FPU: Integrated
CPU(s) enabled: 12 cores, 2 chips, 6 cores/chip
CPU(s) orderable: 1,2 chip
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 256 KB I+D on chip per core
L3 Cache: 15 MB I+D on chip per chip
Other Cache: None
Memory: 128 GB (16 x 8 GB 2Rx4 PC3-14900R-13, ECC, running at 1600 MHz and CL11)
Disk Subsystem: 1 X 300 GB 15000 RPM SAS
Other Hardware: None

Software

Operating System: Red Hat Enterprise Linux Server release 6.4 (Santiago)
 2.6.32-358.el6.x86_64
Compiler: C/C++: Version 14.0.0.080 of Intel C++ Studio XE for Linux
Auto Parallel: Yes
File System: ext4
System State: Run level 3 (multi-user)
Base Pointers: 32-bit
Peak Pointers: 32/64-bit
Other Software: Microquill SmartHeap V10.0



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M3 (Intel Xeon E5-2630L v2, 2.40 GHz)

SPECint2006 = **43.4**

SPECint_base2006 = **41.2**

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Dec-2013
Hardware Availability: Dec-2013
Software Availability: Sep-2013

Results Table

| Benchmark | Base | | | | | | Peak | | | | | |
|----------------|-------------|-------------|------------|-------------|------------|-------------|-------------|-------------|------------|-------------|------------|-------------|
| | Seconds | Ratio | Seconds | Ratio | Seconds | Ratio | Seconds | Ratio | Seconds | Ratio | Seconds | Ratio |
| 400.perlbench | 404 | 24.2 | 403 | 24.2 | 404 | 24.2 | 323 | 30.3 | 322 | 30.3 | 323 | 30.3 |
| 401.bzip2 | 534 | 18.1 | 534 | 18.1 | 533 | 18.1 | 529 | 18.2 | 529 | 18.3 | 529 | 18.2 |
| 403.gcc | 308 | 26.2 | 309 | 26.0 | 310 | 26.0 | 304 | 26.5 | 304 | 26.5 | 306 | 26.3 |
| 429.mcf | 172 | 53.0 | 170 | 53.6 | 170 | 53.5 | 172 | 53.0 | 170 | 53.6 | 170 | 53.5 |
| 445.gobmk | 526 | 19.9 | 527 | 19.9 | 523 | 20.0 | 515 | 20.4 | 515 | 20.4 | 516 | 20.3 |
| 456.hammer | 208 | 44.8 | 245 | 38.0 | 206 | 45.2 | 205 | 45.5 | 205 | 45.5 | 205 | 45.5 |
| 458.sjeng | 544 | 22.2 | 546 | 22.2 | 544 | 22.2 | 567 | 21.3 | 535 | 22.6 | 535 | 22.6 |
| 462.libquantum | 9.97 | 2080 | 9.96 | 2080 | 9.98 | 2080 | 9.97 | 2080 | 9.96 | 2080 | 9.98 | 2080 |
| 464.h264ref | 552 | 40.1 | 553 | 40.0 | 552 | 40.1 | 504 | 43.9 | 504 | 43.9 | 505 | 43.8 |
| 471.omnetpp | 298 | 21.0 | 282 | 22.1 | 282 | 22.2 | 219 | 28.5 | 220 | 28.4 | 220 | 28.4 |
| 473.astar | 290 | 24.2 | 291 | 24.1 | 289 | 24.3 | 290 | 24.2 | 291 | 24.1 | 289 | 24.3 |
| 483.xalancbmk | 157 | 43.9 | 157 | 43.8 | 157 | 43.9 | 158 | 43.6 | 158 | 43.6 | 158 | 43.8 |

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

BIOS Settings:

```

Intel HT Technology = Disabled
CPU performance set to HPC
Power Technology set to Custom
CPU Power State C6 set to Enabled
CPU Power State C1 Enhanced set to Disabled
Energy Performance policy set to Performance
Memory RAS configuration set to Maximum Performance
DRAM Clock Throttling Set to Performance
LV DDR Mode set to Performance-mode
DRAM Refresh Rate Set to 1x
Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6818
$Rev: 6818 $ $Date:: 2012-07-17 #$ e86d102572650a6e4d596a3cee98f191
running on C240M3 Fri Dec 20 03:02:31 2013

```

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
<http://www.spec.org/cpu2006/Docs/config.html#sysinfo>

```

From /proc/cpuinfo
model name : Intel(R) Xeon(R) CPU E5-2630L v2 @ 2.40GHz
2 "physical id"s (chips)
12 "processors"

```

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M3 (Intel Xeon E5-2630L v2, 2.40 GHz)

SPECint2006 = 43.4

SPECint_base2006 = 41.2

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Dec-2013

Hardware Availability: Dec-2013

Software Availability: Sep-2013

Platform Notes (Continued)

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

```
cpu cores : 6
siblings  : 6
physical 0: cores 0 1 2 3 4 5
physical 1: cores 0 1 2 3 4 5
cache size : 15360 KB
```

```
From /proc/meminfo
MemTotal:      132126788 kB
HugePages_Total:    0
Hugepagesize:    2048 kB
```

```
/usr/bin/lsb_release -d
Red Hat Enterprise Linux Server release 6.4 (Santiago)
```

```
From /etc/*release* /etc/*version*
redhat-release: Red Hat Enterprise Linux Server release 6.4 (Santiago)
system-release: Red Hat Enterprise Linux Server release 6.4 (Santiago)
system-release-cpe: cpe:/o:redhat:enterprise_linux:6server:ga:server
```

```
uname -a:
Linux C240M3 2.6.32-358.el6.x86_64 #1 SMP Tue Jan 29 11:47:41 EST 2013 x86_64
x86_64 x86_64 GNU/Linux
```

```
run-level 3 Dec 20 03:00
```

```
SPEC is set to: /opt/cpu2006-1.2
Filesystem      Type      Size  Used Avail Use% Mounted on
/dev/sdal        ext4      275G  34G  227G  13% /
```

```
Additional information from dmidecode:
BIOS Cisco Systems, Inc. C240M3.1.5.3b.0.082020130616 08/20/2013
Memory:
16x 0xAD00 HMT31GR7EFR4C-RD 8 GB 1600 MHz 2 rank
8x NO DIMM NO DIMM
```

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64:/opt/cpu2006-1.2/sh"
OMP_NUM_THREADS = "12"

Binaries compiled on a system with 1x Core i7-860 CPU + 8GB memory using RedHat EL 6.4
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled
runspec command invoked through numactl i.e.:

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M3 (Intel Xeon E5-2630L v2, 2.40 GHz)

SPECint2006 = 43.4

SPECint_base2006 = 41.2

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Dec-2013
Hardware Availability: Dec-2013
Software Availability: Sep-2013

General Notes (Continued)

numactl --interleave=all runspec <etc>

Base Compiler Invocation

C benchmarks:
icc -m64

C++ benchmarks:
icpc -m64

Base Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -DSPEC_CPU_LP64
403.gcc: -DSPEC_CPU_LP64
429.mcf: -DSPEC_CPU_LP64
445.gobmk: -DSPEC_CPU_LP64
456.hmmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX
464.h264ref: -DSPEC_CPU_LP64
471.omnetpp: -DSPEC_CPU_LP64
473.astar: -DSPEC_CPU_LP64
483.xalancbmk: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:
-xSSE4.2 -ipo -O3 -no-prec-div -parallel -opt-prefetch -auto-p32

C++ benchmarks:
-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -auto-p32
-Wl,-z,muldefs -L/sh -lsmartheap64

Base Other Flags

C benchmarks:
403.gcc: -Dalloca=_alloca



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M3 (Intel Xeon E5-2630L v2, 2.40 GHz)

SPECint2006 = 43.4

SPECint_base2006 = 41.2

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Dec-2013

Hardware Availability: Dec-2013

Software Availability: Sep-2013

Peak Compiler Invocation

C benchmarks (except as noted below):

icc -m64

400.perlbench: icc -m32

445.gobmk: icc -m32

464.h264ref: icc -m32

C++ benchmarks (except as noted below):

icpc -m32

473.astar: icpc -m64

Peak Portability Flags

400.perlbench: -DSPEC_CPU_LINUX_IA32

401.bzip2: -DSPEC_CPU_LP64

403.gcc: -DSPEC_CPU_LP64

429.mcf: -DSPEC_CPU_LP64

456.hmmer: -DSPEC_CPU_LP64

458.sjeng: -DSPEC_CPU_LP64

462.libquantum: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX

473.astar: -DSPEC_CPU_LP64

483.xalancbmk: -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:

400.perlbench: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-opt-prefetch -ansi-alias

401.bzip2: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div -prof-use(pass 2) -auto-ilp32
-opt-prefetch -ansi-alias

403.gcc: -xSSE4.2 -ipo -O3 -no-prec-div -inline-alloc
-opt-malloc-options=3 -auto-ilp32

429.mcf: basepeak = yes

445.gobmk: -xSSE4.2(pass 2) -prof-gen(pass 1) -prof-use(pass 2)
-ansi-alias

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M3 (Intel Xeon E5-2630L v2, 2.40 GHz)

SPECint2006 = 43.4

SPECint_base2006 = 41.2

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Dec-2013

Hardware Availability: Dec-2013

Software Availability: Sep-2013

Peak Optimization Flags (Continued)

456.hmmr: -xSSE4.2 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32
-ansi-alias

458.sjeng: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-unroll4

462.libquantum: basepeak = yes

464.h264ref: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-unroll2 -ansi-alias

C++ benchmarks:

471.omnetpp: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-opt-ra-region-strategy=block -ansi-alias
-Wl,-z,muldefs -L/sh -lsmartheap

473.astar: basepeak = yes

483.xalancbmk: -xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -ansi-alias
-Wl,-z,muldefs -L/sh -lsmartheap

Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.html>

<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130717.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.xml>

<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130717.xml>



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M3 (Intel Xeon E5-2630L v2, 2.40 GHz)

SPECint2006 = 43.4

SPECint_base2006 = 41.2

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Dec-2013

Hardware Availability: Dec-2013

Software Availability: Sep-2013

SPEC and SPECint are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.
Report generated on Thu Jul 24 21:05:16 2014 by SPEC CPU2006 PS/PDF formatter v6932.
Originally published on 28 January 2014.